METHODS AND APPARATUS FOR CONTROLLING FORMATION OF DEPOSITS IN A DEPOSITION SYSTEM AND DEPOSITION SYSTEMS AND METHODS INCLUDING THE SAME

Statement of Government Support

The present invention was made, at least in part, with government support under Office of Naval Research Contract No. N00014-02-C-0302. The United States government may have certain rights to this invention.

Field of the Invention

The present invention relates to deposition processes and apparatus and, more particularly, to methods and apparatus for depositing a film on a substrate.

Background of the Invention

Deposition systems and methods are commonly used to form layers such as relatively thin films on substrates. For example, a chemical vapor deposition (CVD) reactor system and process may be used to form a layer of semiconductor material such as silicon carbide (SiC) on a substrate. CVD processes may be particularly effective for forming layers with controlled properties, thicknesses, and/or arrangements such as epitaxial layers. Typically, in a deposition system, such as a CVD system, the substrate is placed in a chamber and a process gas including reagents or reactants to be deposited on the substrate is introduced into the chamber adjacent the substrate. The process gas may be flowed through the reaction chamber in order to provide a uniform or controlled concentration of the reagents or reactants to the substrate. Undesirably, the reagents or reactants may tend to deposit on interior surfaces of the reaction chamber as well. Such deposits may be referred to as "parasitic" deposits because they remove reagents or reactants from the process.

With reference to **Figure 5**, an exemplary conventional deposition system **40** is shown therein and illustrates the process by which deposits may be formed on unintended surfaces of a reaction chamber. The system **40** is, for example, a flow through, hot wall, CVD reactor. The system **40** has a top susceptor member **42** and a bottom susceptor member **44**. The system **40** also has a top liner **43** and a bottom liner **45** defining a reaction chamber **47** therebetween. A substrate **20**, such as a wafer, is positioned in the reaction chamber **47** and may be situated on an interior surface of a platter (which may rotate), for example. A process gas is introduced to the reaction chamber **47** at one end, flowed through the reaction chamber **47** past the substrate **20**, and finally exhausted from the reaction chamber **47** at the opposite end. As indicated by the arrows in the reaction chamber **47** as shown in **Figure 5**, as the process gas flows through the reaction chamber **47** a portion of the process gas may contact the substrate **20** as intended and thereby deposit the reagents or reactants on the substrate **20** to form a layer thereon. However, as indicated by the arrows, a portion of the process gas also contacts an interior surface or ceiling **46** of the top liner **43** as well as interior surfaces of the bottom liner **45** and side walls. As a result, parasitic deposits **50** and **52** of the reagents or reactants from the process gas tend to form on the ceiling **46** and the bottom liner **45**, respectively, as well as on the sidewalls. The parasitic deposits on the ceiling **46** may be particularly harmful because they may dislodge and fall onto the substrate **20** during processing, reducing the quality of the formed layer. Moreover, the changing amount of the parasitic deposits may introduce undesirable variations in temperature and gas flow dynamics, thereby influencing the growth of the layer on the substrate **20**. Depletion of the process gas because of the formation of the parasitic deposits may tend to waste reactants, thereby reducing efficiency and growth rate.

Typically, the deposition process is managed to accommodate the formation of parasitic deposits. The cumulative growth time may be limited to reduce the impact of parasitic deposits on product material. After a set time, the susceptor may be cleaned and reconditioned before more production growth runs are attempted. This procedure may limit both the possible length of any single growth run and the number of runs of shorter duration between cleaning cycles. Despite such efforts, parasitic deposits may nonetheless negatively impact product material due to particle formation, process variability and reduced reactant utilization efficiency.

Summary of the Invention

According to embodiments of the present invention, parasitic deposits are controlled in a deposition system for depositing a film on a substrate, the deposition system of the type defining a reaction chamber for receiving the substrate and including a process gas in the reaction chamber and an interior surface contiguous with the reaction chamber. Such control is provided by flowing a buffer gas to form a gas barrier layer between the interior surface and at least a portion of the process gas such that the gas barrier layer inhibits contact between the interior surface and components of the process gas.

According to further embodiments of the present invention, a deposition system for depositing a film on a substrate using a process gas includes a reaction chamber adapted to receive the substrate and the process gas. The system further includes an interior surface contiguous with the reaction chamber. A buffer gas supply system is adapted to supply a flow of a buffer gas between the interior surface and at least a portion of the process gas such that the flow of the buffer gas forms a gas barrier layer to inhibit contact between the interior surface and components of the process gas when the process gas is disposed in the reaction chamber.

According to yet further embodiments of the present invention, a deposition control system is provided for controlling parasitic deposits in a deposition system for depositing a film on a substrate, the deposition system of the type defining a reaction chamber for holding the substrate and including a process gas in the reaction chamber and an interior surface contiguous with the reaction chamber. The deposition control system includes a buffer gas supply system adapted to provide a flow of a buffer gas between the interior surface and at least a portion of the process gas such that the flow of the buffer gas forms a gas barrier layer to inhibit contact between the interior surface and components of the process gas.

According to further embodiments of the present invention, a deposition system for depositing a film on a substrate includes a reaction chamber adapted to receive the substrate and an interior surface contiguous with the reaction chamber. A process gas is disposed within the reaction chamber. A flow of a buffer gas is disposed between the interior surface and at least a portion of the process gas. The flow of the buffer gas forms a gas barrier layer to inhibit contact between the interior surface and components of the process gas.

According to further embodiments of the present invention, a susceptor assembly for depositing a film on a substrate using a process gas and a buffer gas each flowed in a flow direction includes at least one susceptor member. The at least one susceptor member defines a reaction chamber, a process gas inlet and a buffer gas inlet. The reaction chamber is adapted to receive the substrate and has a buffer gas region to receive the buffer gas. The reaction chamber has a first cross-sectional area perpendicular to the flow direction. The process gas inlet has a second cross-sectional area perpendicular to the flow direction. The second cross-sectional area is less than the first cross-sectional area. The buffer gas inlet is adjacent the process gas inlet and is adapted to direct the buffer gas into the buffer gas region of the reaction chamber.

Brief Description of the Drawings

Figure 1 is a schematic view of a deposition system according to embodiments of the present invention;

Figure 2 is a perspective view of a susceptor assembly forming a part of the deposition system of **Figure 1**;

Figure 3 is a cross-sectional view of the susceptor assembly of **Figure 2** taken along the line **3-3** of **Figure 2**, wherein a buffer gas supply line, a substrate, a flow of buffer gas and a flow of process gas are also shown;

Figure 4 is a rear end elevational view of the susceptor assembly of **Figure 2** and the substrate; and

Figure 5 is a schematic view of a conventional deposition system.

Detailed Description of the Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the relative sizes of regions or layers may be exaggerated for clarity. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

With reference to **Figure 1**, a deposition system **101** according to embodiments of the present invention is schematically shown therein. The deposition system **101** may be a horizontal, hot wall, flow through, CVD system as shown including a susceptor assembly **100**, a quartz tube **180** defining a through passage **180A**, an electromagnetic frequency (EMF) generator **182** (for example, including a power supply and an RF coil surrounding the tube **180**) and a process gas supply system **161**. An insulative cover may be provided about the susceptor assembly **100** in addition to or in place of the quartz tube **180**. The deposition system **101** further includes a buffer gas supply system **171** in accordance with the present invention. The deposition system **101** may be used to form a layer or film on a substrate **20** (**Figure 3**). While only a single substrate **20** is illustrated in **Figures 3** and **4**, the system **101** may be adapted to form films concurrently on multiple substrates **20**.

The substrate **20** may be a wafer or other structure formed of the same or a different material than that of the layer to be deposited. The substrate **20** may be formed of, for example, SiC, sapphire, a Group III nitride, silicon, germanium, and/or a III-V or II-VI compound or interalloy, or the like. The substrate surface upon which the film is deposited may be a base substrate or a first or subsequent layer superimposed on a base substrate. For example, the surface of the substrate **20** for receiving the deposited film may be a layer previously deposited using the deposition system **101** or an alternative apparatus. As will be appreciated by those of skill in the art in light of the present disclosure, embodiments of the present invention may be advantageously utilized with semiconductor materials other than those specifically mentioned herein. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group IIIA of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds such as AlGaN and AlInGaN. As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (*e.g.*, GaN), ternary (*e.g.*, AlGaN, AlInN), and quaternary (*e.g.*, AlInGaN) compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the Group III elements. Accordingly, formulas such as $Al_xGa_{1-x}N$ where $0 \leq x \leq 1$ are often used to describe them.

Generally, the process gas supply system **161** supplies a process gas into and through the susceptor assembly **100** as discussed below. The EMF generator **182** inductively heats the susceptor assembly **100** to provide a hot zone in the susceptor assembly **100** where deposition reactions take place. The process gas continues through and out of the susceptor assembly **100** as an exhaust gas which may include remaining components of the process gas as well as reaction by-products, for example. Embodiments of the present invention may be used in types of deposition systems other than hot wall CVD systems. Other modifications to the systems and methods of the present invention will be apparent to those of ordinary skill in the art upon reading the description herein.

The process gas supply system **161** includes a supply **160** of the process gas. The process gas includes one or more components such as reagents, reactants, species, carriers and the like. One or more of these components may be capable, alone or in combination with one or more other components (which may also be present in the process gas), of forming deposits on a surface such as the ceiling or interior surface **120** (**Figure 3**). Exemplary components that may form or assist in forming deposits upon contacting the ceiling surface **120** include SiH_4, C_3H_8, C_2H_4, Si_2H_6, $SiCl_4$, SiH_2Cl_2, $SiCl_3(CH_3)$, NH_3, trimethyl gallium, and trimethyl aluminum. Where it is desired to form a SiC layer on a substrate, the process gas may include precursor gases such as silane (SiH_4) and propane (C_3H_8) along with a carrier gas such as purified hydrogen gas (H_2). The process gas supply **160** may be provided from one or more pressurized containers of the gases with flow control and/or metering devices as needed. The process gas may be adapted to deposit a layer of SiC, a Group III nitride, silicon, germanium, and/or a III-V and/or II-VI compound or interalloy on the substrate **20**.

The buffer gas supply system **171** includes a supply **170** of a buffer gas fluidly connected to the susceptor assembly **100** by a line **172**. The buffer gas supply **170** may be provided from one or more pressurized canisters of the gas or gases with flow control and/or metering devices as needed. A heater **174** may be provided along the line **172**, in or at the susceptor assembly **100**, or at the buffer gas supply **160** for preheating the buffer gas.

The buffer gas may be any suitable gas. According to some embodiments, the buffer gas is a gas having relatively low diffusion rates for many or selected ones of the species or components present in the process gas. According to some embodiments, the buffer gas is a noble gas. The noble gas may include argon, helium, neon, krypton, radon, or xenon. Other suitable gases include H_2, N_2, NH_3 or air. The buffer gas may include or be substantially composed of a species capable of chemically assisting in removing or inhibiting deposits of reactants from the process gas. For example, in accordance with some embodiments and particularly in the case of a process for growing a layer of SiC on a substrate, the buffer gas includes an etchant such as HCl, Cl_2 and/or a carbon-containing gas such as propane.

Turning to the susceptor assembly **100** in greater detail and with reference to **Figures 2** to **4** the susceptor assembly **100** includes a top member **110**, a pair of side members **130**, and a bottom member **140**. The susceptor assembly **100** extends from an entrance end **100A** to an exit end **100B**. The members **110, 130, 140** define an entrance opening **102** (at the end **100A**) and an exit opening **104** (at the end **100B**). The members **110, 130, 140** also define a reaction chamber **106** extending from a process gas inlet **102B** to the opening **104**. According to some embodiments, the reaction chamber **106** has a length of between about 0.1 and 1 meter, a width of between about 0.05 and 0.5 meter, and a height of between about 1 and 10 cm.

The top member **110** includes a core or susceptor body **112** covered (and preferably substantially fully surrounded) by a layer **114**. The layer **114** includes the ceiling or interior surface **120** facing and contiguous with the reaction chamber **106**.

The core **112** is preferably formed of a susceptor material suitable to generate heat responsive to eddy currents generated therein by the EMF generator **182**, such materials and inductive heating arrangements being well known to those of skill in the art. The core **112** may be formed of graphite, and more preferably of high purity graphite.

The layer **114** may be formed of a material having high purity and which is able to withstand the process temperatures (typically in the range of 1500 to 1800°C for SiC deposition). The layer **114** may be formed of, for example, SiC or a refractory metal carbide such as TaC, NbC and/or TiC. The layer **114** may be applied to the core **112** by any suitable method. Preferably, the layer **114** is a dense, impervious coating and has a thickness of at least about 10μm, and more preferably, between about 20μm and 100μm.

The top member **110** further includes a downwardly stepped portion **116** adjacent the opening **102**. The stepped portion **116** and the underlying portion of the liner **152** define the process gas inlet **102B** and a process gas inlet passage **102A** extending from the opening **102** to the process gas inlet **102B**. The step portion **116** also defines a buffer gas region **106A** (**Figure 3**) in the upper portion of the reaction chamber **106**.

A plurality of passages **117** (one shown in **Figure 3**) extend through the top member **110** and terminate at a respective port **176** (see **Figures 3** and **4**). A common feed inlet **117A** (**Figures 2** and **3**) is provided for connecting the buffer gas line **172** to the passages **117** which may be interconnected in a manifold arrangement by a lateral passage **117B** (**Figure 3**). Alternatively, separate lines and/or inlets may be provided for some or each of the ports **176**. The passages **117**, the inlet **117A** and the ports **176** may be formed in the top member **110** by any suitable method such as drilling or molding.

The bottom member **140** includes a core **142** covered by a coating or layer **144**. Suitable materials and methods for forming the core **142** and the layer **144** are as described above for the core **112** and the layer **114**. The side members **130** similarly include respective cores (not shown) and covering layers which may be formed of the same materials and using the same methods as described above for the core **112** and the layer **114**.

A liner or liners **152** may overlie the bottom member **140** as shown in **Figures 3** and **4**. The liner **152** may be formed of SiC or SiC coated graphite, for example, as disclosed in U.S. Patent Application Serial No. 10/017,492, filed October 20, 2001, the disclosure of which is incorporated herein by reference.

A platter **154** or the like may be situated between the bottom member **140** and the substrate **20** to support the substrate **20**. According to some embodiments, the platter **154** may be rotatively driven by a suitable mechanism (not shown). For example, the system may include a gas-driven rotation system as described in Applicant's U.S. Application Serial No. 09/756,548, titled *Gas Driven Rotation Apparatus and Method for Forming Silicon Carbide Layers*, filed January 8, 2001, and/or as described in Applicant's U.S. Application Serial No. 10/117,858, titled *Gas Driven Planetary Rotation Apparatus and Methods for Forming Silicon Carbide Layers*, filed April 8, 2002, the disclosures of which are hereby incorporated herein by reference in their entireties. Alternatively, the platter **154** may be stationary. The platter **154** may be adapted to hold one or multiple substrates **20**. The platter **154** may be formed of any suitable material such as SiC coated graphite, solid SiC or solid SiC alloy. The platter **154** may be omitted such that the substrate rests on the bottom member **140**, the liner **152**, or other suitable support.

In use, the process gas supply system **161** supplies a flow of the process gas to the reaction chamber **106** through the inlet opening **102**. The process gas **P** flows generally in a flow direction **R** (**Figure 3**). The arrows labeled **P** in **Figure 3** indicate the general flow path of the process gas and the reagents therein. As shown, the process gas and the reagents therein contact the substrate **20** to form the desired layer (e.g., an epilayer) on the exposed surface of the substrate **20**.

Concurrently, the buffer gas supply system **171** supplies or inserts a flow of the buffer gas into the buffer gas region **106A** of the reaction chamber **106** through the ports **176** such that the buffer gas **B** flows through the reaction chamber **106** generally in the flow direction **R**. The arrows labeled **B** in **Figure 3** indicate the general flow path of the flow of buffer gas. The buffer gas **B** flows in the buffer gas region **106A** along the ceiling or interior surface **120** so as to form a barrier layer **178** of flowing buffer gas extending upwardly from the dashed line of **Figure 3** to the ceiling surface **120**.

The barrier layer **178** serves to inhibit or impede the movement of the process gas **P** and components thereof from moving into contact with the ceiling surface **120** where reagents or reactants of the process gas **P** might otherwise form deposits. Below the barrier layer **178**, the process gas **P** is permitted to flow in the normal manner to, over and beyond the substrate **20**. In this manner, the process gas **P** and the deposition system **101** form the desired layer(s) on the exposed surface(s) of the substrate **20**. The flow of buffer gas **B** may also serve to push the reactant stream of the process gas **P** toward the substrate **20**, thereby accelerating the growth rate.

As discussed in more detail below, according to some embodiments, the buffer gas **B** flow is maintained as a substantially laminar flow. As long as the flow of the buffer gas **B** is laminar, the only way reagents or other components from the process gas **P** can reach the ceiling surface is by diffusing from the process gas **P** flow and through the barrier gas **B** flow. In general, the distance **S** a diffusing species will traverse during time span of t follows the relationship **S** $\approx \sqrt{Dt}$, where D is the diffusion rate. In the present case, t is the transit time of species through the reaction chamber **106**. The transit distance of concern will depend on to what lengthwise extent the operator or designer desires to inhibit deposits downstream of the process gas inlet **102B**. In most cases, it will be deemed sufficient to inhibit or prevent the formation of deposits on the ceiling surface **120** up to the downstream edge of the substrate **20**. In the susceptor assembly **100** illustrated in **Figure 3**, this transit distance is indicated by the distance **L**. The transit time can generally be determined as follows:

$$t \approx \frac{L}{\left(\frac{M}{\rho A}\right)}$$

Where :

L = Length of susceptor

M = Mass flow rate

ρ = Average density of gas within susceptor, determined by pressure, temperature and gas composition.

A = Cross sectional area of susceptor opening.

In order for the barrier layer **178** to prevent all diffusion of the components of the process gas **P**, the thickness **S** of the barrier layer **178** (which may correspond generally to the height **I** of the step portion **116**) should satisfy:

$$S \geq \sqrt{Dt} = \sqrt{\frac{DL}{\left(\frac{M}{\rho A}\right)}}$$

It will be appreciated by those of ordinary skill in the art upon reading the description herein that, in accordance with the present invention, it is not necessary to completely prevent all components of the process gas **P** from contacting the ceiling surface **120** as may be accomplished by providing fully laminar flow of the buffer gas **B** and a barrier layer **178** having a thickness **S** satisfying the foregoing criteria. Rather, the system **101** may be designed to allow some turbulence and/or have a barrier layer thickness **S** less than that necessary to preclude all deposits. In this manner, for example, the system **101** may provide a significant reduction in parasitic deposits while allowing some deposits to occur. According to some embodiments, the rate of formation of parasitic deposits on the ceiling surface **120** is preferably no more than one half the growth rate on the substrate **20** and more preferably no more than one quarter the growth rate on the substrate **20**.

The barrier layer thickness **S** may be increased to provide an additional margin of protection for the ceiling surface **120** or to compensate for turbulence in the buffer gas flow **B**. The height of the buffer gas region **106A** may be greater than, less than, or the same as the optimal thickness **S** of the barrier layer **178**.

Further, various process parameters may be considered in determining the degree of laminarity of the buffer gas **B** flow and the distance **S** needed to obtain the desired reduction or prevention of deposits on the ceiling surface **120**. For example, at typical SiC epilayer growth temperatures (i.e., in the range of about 1500 to 1800°C), simultaneous etch and deposition processes may take place. Therefore, for a given growth condition, there may exist a critical minimum reagent supply rate necessary to stabilize the surface (in this case, the ceiling surface 120). A reagent supply rate above critical will result in growth of parasitic deposits on the ceiling surface **120** while a supply rate below critical will result in etching of parasitic deposits from the ceiling surface **120**. Accordingly, even if the reagent flux to the ceiling were only reduced to the critical supply rate, then essentially no net deposition would occur on the ceiling.

Preferably, the deposition system **101** is adapted to maintain the flow of the buffer gas **B** and the flow of the process gas **P** as a laminar flow to at least a location downstream of the substrate **20**, and more preferably, throughout the reaction chamber **106**, to reduce or prevent mixing or turbulence between the flows that may promote transport of the process gas **P** through the barrier layer **178**.

The relative dimensions and configurations of the reaction chamber **106**, the process gas inlet **102B**, and the buffer gas ports **176** may be selected to promote laminar flow. According to some embodiments and as illustrated (see **Figures 3** and **4**), the process gas inlet **102B** is smaller in cross-section (i.e., generally perpendicular to the flow direction **R** of the gases, and as shown in **Figure 4**) than the reaction chamber **106** so that a remaining space (i.e., the buffer gas region **106A**) is available in the reaction chamber **106** for insertion of the buffer gas **B** into the reaction chamber **106** without inserting the buffer gas **B** into the process gas or into the unmodified flow path of the process gas **P**.

In the illustrated embodiment, the provision of the stepped portion **116** may facilitate laminar flow. According to some embodiments of the present invention, the sum of the height **G** of the opening **102** and the height **I** of the step portion **116** is substantially the same as the full height **H** of the reaction chamber **106** (see **Figure 3**). Preferably, the widths of the process gas inlet **102B**, the step portion **116**, and the reaction chamber **106** are substantially the same so that the cross-sectional area (i.e., generally perpendicular to the flow direction **R** of the gases, and as shown in **Figure 4**) of the reaction chamber **106** is substantially the same as the combined cross-sectional area of the process gas inlet **102B** and the step portion **116**. In this manner, the flow of the process gas **P** and the flow of the buffer gas **B** enter the reaction chamber **106**, in parallel, at substantially the same axial location in the reaction chamber **106** along the direction of flow **R** of the gases **P**, **B**. Because the buffer gas region **106A** is provided above the natural flow path of the process gas **P**, the buffer gas **B** can be inserted into the reaction chamber **106** without substantially displacing the process gas **P**. As a result, turbulence and mixing of the gas flows that might otherwise be created by initially introducing the buffer gas **B** into the path of the process gas **P** may be avoided. The height **I** of the step portion **116** is preferably between about 5 and 25% of the height **H** of the reaction chamber **106**.

According to some embodiments and as illustrated, the reaction chamber **106** has a substantially uniform height **H** along substantially its full length. In this case, the reaction chamber **106** may have a substantially uniform cross-sectional area along its full length. This configuration may serve to promote the integrity of the boundary layer between the flow of the process gas **P** and the flow of the buffer gas **B**. The height **H** of the reaction chamber **106** is preferably between about 0.5 and 5 cm. According to further embodiments, the height **H** is not uniform, but rather the ceiling is tilted or curved in either direction to improve uniformity or efficiency of the process. In this case, the cross-sectional area of the reaction chamber **106** may vary, uniformly or non-uniformly.

While a step portion **116** and ports **176** are shown and described, other features and geometries may be used to control the flow of the buffer gas **B** so as to control turbulence in the flow of the buffer gas **B**. The configurations of the process gas inlet passage **102A**, the process gas inlet **102B**, the inlet opening **102**, the buffer gas passages **117**, and/or the buffer gas inlets **176** may be adapted to promote laminar flow of and between the process gas **P** and the buffer gas **B**. The axial length **K** (**Figure 3**) of the process gas inlet passage **102A** may be extended to reduce turbulence in the process gas **P** entering through the inlet **102** before the process gas **P** enters the reaction chamber **106** through the process gas inlet **102B**. However, because the passage **102A** is within the susceptor assembly **100** and is thus heated, reactions may occur which tend to form deposits or the ceiling surface of the passage **102A**. For this reason, it may be desirable to minimize the length of the passage **102A**. The buffer gas ports **176** may be replaced with one or more suitably configured slots.

According to some embodiments, the velocity of the process gas **P** and the velocity of the buffer gas **B** through the reaction chamber **106** are substantially the same. For SiC epitaxy, in accordance with some embodiments of the present invention where the length of the reaction chamber **106** is between about 0.1 and 1 m, the velocity of the gases **P, B** is at least about 1 m/s, and preferably between about 5 and 100 m/s to limit the time for diffusion of the process gas **P** through the barrier layer **178**.

In order to further promote the integrity of the barrier layer **178** and thereby inhibit diffusion of the process gas **P** therethrough, the buffer gas **B** may be provided at a temperature greater than the temperature of the adjacent process gas **P**. The hotter buffer gas **B** will naturally segregate from the relatively cooler process gas **P** along the ceiling surface **120** because of the relative buoyancy of the hotter gas. According to some embodiments, the average temperature of the buffer gas **B** is at least 10°C hotter than the average temperature of the process gas in the reaction chamber **106**.

The buffer gas **B** may be heated using the heater **174**. Additionally or alternatively, the buffer gas **B** may be heated by heating the ceiling surface **120** to a temperature greater than the temperature or temperatures of the lower surfaces contiguous with the reaction chamber **106** which the process gas **P** contacts, i.e., by providing a temperature differential between the ceiling surface **120** and the floor, the platter **154** and/or other surfaces contacting the process gas **P**. That is, the temperature profile in the reaction chamber **106** may be deliberately and selectively maintained as spatially non-uniform (e.g., as a gradient) extending from the ceiling surface **120** to the lower and/or other surfaces contiguous with the reaction chamber **106**. This may be accomplished, for example, by providing greater thermal insulation between the core **142** and the surfaces of the liner **152**, the platter **154** and the substrate **20** contacting the process gas **P** than is provided between the core **112** and the ceiling surface **120**. For example, the liner **152** and the layer **114** may be suitably relatively constructed (e.g., by selection of material and thickness) to provide desired relative insulative effects. Because the top member **110** and the bottom member **140** are inductively heated, primarily by the resistivity of their graphite cores **112**, **142**, the temperatures of the surfaces of the liner **152**, the platter **154** and the substrate **20** contacting the process gas **P** are thereby reduced as compared to the temperature of the ceiling surface **120**. The buffer gas **B** is thus heated at a faster rate than the process gas **P**. To promote conduction of heat from the core **112** to the ceiling surface **120**, the layer **114** may be directly coated on the core **112** to form a relatively monolithic or unitary top member **110**.

Alternatively or additionally, a temperature differential can be created or increased between the ceiling surface **120** and the other surfaces such as the liner **152** or other lower surfaces by forming the layer **114** (and thus the ceiling surface **120**) from a material having a lower emissivity than the material of the layer **144** and/or of the liner **152** or other surfaces contacting the process gas **P** stream. For example, the layer **114** may be formed of TaC (which has an emissivity of about 0.4) and the liner **152** and the platter **154** may be formed of SiC (which has an emissivity of about 0.9). As a result, the layer **114**, and therefore the ceiling surface **120**, will lose comparatively less heat from radiation, resulting in a higher temperature at the ceiling surface **120**. Moreover, parasitic deposits may tend to adhere less well to TaC or other metal carbides than to SiC. As a further advantage, in many applications, a TaC coating will typically be more durable than a SiC coating, which may serve to prolong the service life of the part.

In addition to the barrier effect, the ceiling surface **120** can be heated, for example, in one or more of the manners described above, such that it is sufficiently hotter than the other components in the reaction chamber **106** to induce etching or sublimation of deposits on the ceiling surface **120**. That is, deposits on the relatively hot ceiling surface **120** will tend to etch away or sublime and return to the buffer gas **B** or the process gas **P** rather than remaining on the ceiling surface **120**.

As discussed above, the buffer gas **B** may consist of or include HCl or other active gas to chemically impede the formation of parasitic deposits on the ceiling surface **120** and/or to remove such deposits.

Because the growth of parasitic deposits on the ceiling surface **120** is inhibited or suppressed, greater volumes of process gas **P** can be flowed through the reaction chamber **106** before cleaning or the like is required. Deposition systems and methods in accordance with the present invention may greatly extend the permissible growth time and layer thickness while improving repeatability and efficiency. Moreover, the reduction in the rate of deposit formation may allow the use of lower ceiling heights, which allows for more efficient use of the process gas and improved thermal uniformity.

While the foregoing deposition system **101** and methods are described as relating to a horizontal, hot wall, CVD, flow through deposition process, various aspects of the present invention may be used in other types of deposition systems and processes. While particular embodiments have been described with reference to "top", "bottom" and the like, other orientations and configurations may be employed in accordance with the invention. For example, the deposition system and process may be a cold wall and/or non-horizontal flow through system and process. The deposition system and process may be a vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), or plasma enhanced CVD (PECVD) deposition system and process rather than a CVD system or process. The present invention is not limited to providing a barrier layer for a ceiling surface of a reaction chamber. The buffer gas supply system may be modified to provide a buffer gas flow along one or more surfaces in addition to or instead of the ceiling surface. For example, the buffer gas supply system may be employed to inhibit parasitic deposits from forming on a lower liner or other surfaces upstream from the substrate **20**, or in other locations where parasitic deposits are problematic.

While the systems and methods have been described in relation to processes for depositing layers on substrates such as semiconductor wafers, the present invention may be employed in processes for depositing layers or the like on other types of substrates. The systems and methods of the present invention may be particularly useful in processes for forming an epitaxial layer on a substrate.

Various other modifications may be made in accordance with the invention. For example, the reaction chamber may be closed at one or both ends rather than providing a through passage. Heating systems may be used other than or in addition to inductive heating.

As used herein a "system" may include one or multiple elements or features. In the claims that follow, the "deposition system", the "deposition control system", the "buffer gas supply system", the "process gas supply system" and the like are not limited to systems including all of the components, aspects, elements or features discussed above or corresponding components, aspects, elements or features.

The foregoing is illustrative of the present invention and is not to be construed as limiting thereof. Although a few exemplary embodiments of this invention have been described, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the invention.

THAT WHICH IS CLAIMED IS:

1. A method for controlling parasitic deposits in a deposition system for depositing a film on a substrate, the deposition system of the type defining a reaction chamber for receiving the substrate and including a process gas in the reaction chamber and an interior surface contiguous with the reaction chamber, the method comprising:

flowing a buffer gas to form a gas barrier layer between the interior surface and at least a portion of the process gas, such that the gas barrier layer inhibits contact between the interior surface and components of the process gas.

2. The method of Claim 1 wherein the step of flowing the buffer gas includes flowing the buffer gas along the interior surface.

3. The method of Claim 1 including flowing the process gas through the reaction chamber in a flow direction, and wherein the step of flowing the buffer gas includes flowing the buffer gas through the reaction chamber in the flow direction.

4. The method of Claim 3 wherein the step of flowing the buffer gas includes flowing the buffer gas through the reaction chamber at substantially the same velocity as the process gas.

5. The method of Claim 3 including introducing both the buffer gas and the process gas into the reaction chamber at substantially the same location along the flow direction so as to inhibit turbulence in and mixing between their respective flows.

6. The method of Claim 1 including flowing the process gas into the reaction chamber through a process gas inlet, and wherein:

the process gas inlet has a smaller cross-sectional area than a cross-sectional area of the reaction chamber so as to define a buffer gas region in the reaction chamber; and

the step of flowing the buffer gas includes flowing the buffer gas into the buffer gas region.

7. The method of Claim 1 wherein the step of flowing the buffer gas includes providing a substantially laminar flow of the buffer gas along the interior surface.

8. The method of Claim 1 wherein the interior surface overlies the substrate.

9. The method of Claim 1 including providing the buffer gas to the reaction chamber at temperature greater than a temperature of the process gas in the reaction chamber.

10. The method of Claim 9 including heating the buffer gas before introducing the buffer gas into the reaction chamber.

11. The method of Claim 9 including heating the buffer gas as the buffer gas flows along the interior surface.

12. The method of Claim 1 including heating the interior surface to a temperature sufficient to promote sublimation of parasitic deposits from the process gas that deposit on the interior surface.

13. The method of Claim 1 including inductively heating a susceptor member adjacent the interior surface to thereby heat the interior surface.

14. The method of Claim 1 wherein the step of flowing the buffer gas includes flowing the buffer gas through the reaction chamber at a velocity of at least about 1 m/s.

15. The method of Claim 14 wherein the step of flowing the buffer gas includes flowing the buffer gas through the reaction chamber at a velocity of between about 5 and 100 m/s

16. The method of Claim 1 wherein the buffer gas comprises a noble gas.

17. The method of Claim 16 wherein the noble gas is selected from the group consisting of argon, helium, neon, krypton, radon, and xenon.

18. The method of Claim 1 wherein the buffer gas comprises H_2, N_2, NH_3 and/or air.

19. The method of Claim 1 wherein the buffer gas includes an active material capable of chemically inhibiting the deposition of parasitic deposits on the interior surface and/or removing parasitic deposits from the interior surface.

20. The method of Claim 19 wherein the active material includes an etchant.

21. The method of Claim 20 wherein the etchant includes at least one of HCl, Cl_2 and a carbon-containing gas.

22. The method of Claim 1 wherein the deposition system is a chemical vapor deposition (CVD) system.

23. The method of Claim 22 wherein the deposition system is a hotwall CVD system.

24. The method of Claim 1 wherein the substrate is a semiconductor substrate.

25. The method of Claim 24 wherein the substrate comprises a material selected from the group consisting of SiC, sapphire, a Group III nitride, silicon, germanium, and III-V and II-VI compounds and interalloys.

26. The method of Claim 1 wherein the process gas comprises a reagent selected from the group consisting of SiH_4, C_3H_8, C_2H_4, Si_2H_6, $SiCl_4$, SiH_2Cl_2, $SiCl_3(CH_3)$, NH_3, trimethyl gallium, and trimethyl aluminum.

27. The method of Claim 1 wherein the process gas is adapted to deposit onto the substrate a layer of material selected from the group consisting of SiC, a Group III nitride, silicon, germanium, and III-V and II-VI compounds and interalloys.

28. A deposition system for depositing a film on a substrate using a process gas, the deposition system comprising:

a) a reaction chamber adapted to receive the substrate and the process gas;

b) an interior surface contiguous with the reaction chamber; and

c) a buffer gas supply system adapted to supply a flow of a buffer gas between the interior surface and at least a portion of the process gas such that the flow of the buffer gas forms a gas barrier layer to inhibit contact between the interior surface and components of the process gas when the process gas is disposed in the reaction chamber.

29. The system of Claim 28 wherein the buffer gas supply system is adapted to flow the buffer gas along the interior surface.

30. The system of Claim 28 including a process gas supply system to supply a flow of the process gas to the reaction chamber.

31. The system of Claim 30 wherein:

the process gas supply system is adapted to supply the flow of the process gas through the reaction chamber in a flow direction; and

the buffer gas supply system is adapted to flow the buffer gas through the reaction chamber in the flow direction.

32. The method of Claim 31 wherein the buffer gas supply system and the process gas supply system are adapted to flow the buffer gas and the process gas through the reaction chamber at substantially the same velocity.

33. The system of Claim 30 wherein the buffer gas supply system and the process gas supply system are adapted to introduce both the buffer gas and the process gas into the reaction chamber at substantially the same location along the flow direction so as to inhibit turbulence in and between the buffer gas flow and the process gas flow.

34. The system of Claim 30 including a process gas inlet to supply the process gas to the reaction chamber, wherein:

the process gas inlet has a smaller cross-sectional area than a cross-sectional area of the reaction chamber so as to define a buffer gas region in the reaction chamber; and

the buffer gas supply system is adapted to flow the buffer gas into the buffer gas region.

35. The system of Claim 28 wherein the buffer gas supply system is adapted to provide a substantially laminar flow of the buffer gas along the interior surface.

36. The system of Claim 28 wherein the interior surface is a ceiling surface of the reaction chamber.

37. The system of Claim 28 adapted to provide the buffer gas to the reaction chamber at a temperature greater than a temperature of the process gas in the reaction chamber.

38. The system of Claim 37 wherein the buffer gas supply system is adapted to heat the buffer gas before introducing the buffer gas into the reaction chamber.

39. The system of Claim 37 adapted to heat the buffer gas as the buffer gas flows along the interior surface.

40. The system of Claim 28 adapted to heat the interior surface to a temperature sufficient to promote sublimation of parasitic deposits from the process gas that deposit on the interior surface.

41. The system of Claim 28 wherein the buffer gas supply system is adapted to flow the buffer gas through the reaction chamber at a velocity of at least about 1 m/s.

42. The system of Claim 41 wherein the buffer gas supply system is adapted to flow the buffer gas through the reaction chamber at a velocity of between about 5 and 100 m/s.

43. The system of Claim 28 wherein the buffer gas supply system includes a supply of buffer gas.

44. The system of Claim 43 wherein the buffer gas comprises a noble gas.

45. The system of Claim 44 wherein the noble gas is selected from the group consisting of argon, helium, neon, krypton, radon, and xenon.

46. The system of Claim 43 wherein the buffer gas comprises H_2, N_2, NH_3 and/or air.

47. The system of Claim 43 wherein the buffer gas includes an active material capable of chemically inhibiting the deposition of parasitic deposits on the interior surface and/or removing parasitic deposits from the interior surface.

48. The system of Claim 47 wherein the active material includes an etchant.

49. The system of Claim 48 wherein the etchant includes at least one of HCl, Cl_2 and a carbon-containing gas.

50. The system of Claim 28 wherein the system is a chemical vapor deposition (CVD) system.

51. The system of Claim 50 wherein the system is a hotwall CVD system.

52. The system of Claim 28 adapted to heat the interior surface to a higher temperature than a second surface that is adapted to contact the process gas when the process gas is disposed in the reaction chamber.

53. The system of Claim 52 wherein the second surface comprises a first material and the interior surface comprises a second material, the second material having a lower emissivity than the first material.

54. The system of Claim 53 wherein the second surface is formed of SiC and the interior surface is formed of a metal carbide.

55. The system of Claim 54 wherein the second surface is formed of at least one of TaC and NbC.

56. The system of Claim 53 including at least one susceptor member responsive to an eddy current to heat each of the interior surface and the second surface.

57. A deposition control system for controlling parasitic deposits in a deposition system for depositing a film on a substrate, the deposition system of the type defining a reaction chamber for receiving the substrate and including a process gas in the reaction chamber and an interior surface contiguous with the reaction chamber, the deposition control system comprising:

a buffer gas supply system adapted to provide a flow of a buffer gas between the interior surface and at least a portion of the process gas such that the flow of the buffer gas forms a gas barrier layer to inhibit contact between the interior surface and components of the process gas.

58. A deposition system for depositing a film on a substrate, the deposition system comprising:

a) a reaction chamber adapted to receive the substrate;

b) an interior surface contiguous with the reaction chamber;

c) a process gas disposed within the reaction chamber; and

d) a flow of a buffer gas disposed between the interior surface and at least a portion of the process gas, the flow of the buffer gas forming a gas barrier layer to inhibit contact between the interior surface and components of the process gas.

59. A susceptor assembly for depositing a film on a substrate using a process gas and a buffer gas each flowed in a flow direction, the susceptor assembly comprising at least one susceptor member defining:

a) a reaction chamber adapted to receive the substrate and having a buffer gas region to receive the buffer gas, the reaction chamber having a first cross-sectional area perpendicular to the flow direction; and

b) a process gas inlet having a second cross-sectional area perpendicular to the flow direction, the second cross-sectional area being less than the first cross-sectional area; and

c) a buffer gas inlet adjacent the process gas inlet and adapted to direct the buffer gas into the buffer gas region of the reaction chamber.

60. The susceptor assembly of Claim 59 wherein:

the buffer gas region has a third cross-sectional area perpendicular to the flow direction; and

the third cross-sectional area and the second cross-sectional area have a combined cross-sectional area that is substantially the same as the first cross-sectional area.

61. The susceptor assembly of Claim 59 wherein the at least one susceptor member includes a step portion and the buffer gas inlet is formed in the step portion.

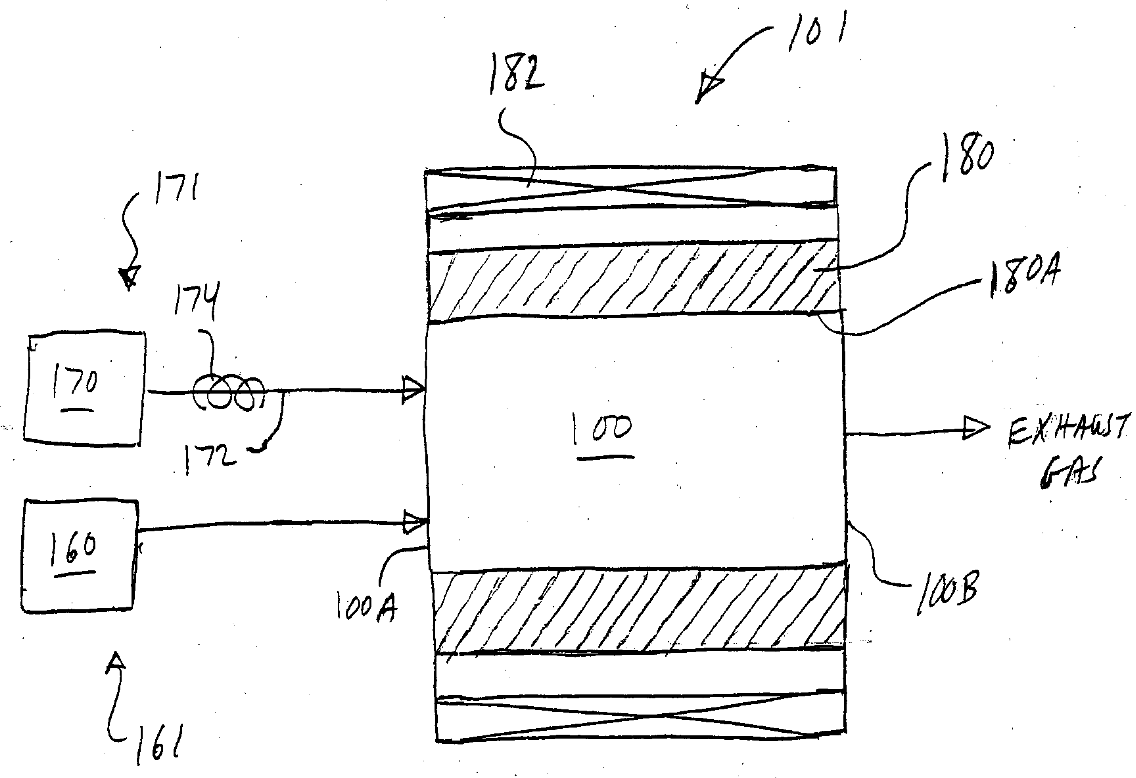
62. The susceptor assembly of Claim 59 wherein the reaction chamber has a length extending along the flow direction and the cross-sectional area of the reaction chamber is substantially uniform along substantially the entirety of the length of the reaction chamber.

63. The susceptor assembly of Claim 59 wherein the reaction chamber has a length extending along the flow direction and the cross-sectional area of the reaction chamber is non-uniform along the length of the reaction chamber.

METHODS AND APPARATUS FOR CONTROLLING FORMATION OF DEPOSITS IN A DEPOSITION SYSTEM AND DEPOSITION SYSTEMS AND METHODS INCLUDING THE SAME

Abstract

Parasitic deposits are controlled in a deposition system for depositing a film on a substrate, the deposition system of the type defining a reaction chamber for receiving the substrate and including a process gas in the reaction chamber and an interior surface contiguous with the reaction chamber. Such control is provided by flowing a buffer gas between the interior surface and at least a portion of the process gas to form a gas barrier layer such that the gas barrier layer inhibits contact between the interior surface and components of the process gas. A deposition system for depositing a film on a substrate using a process gas includes a reaction chamber adapted to receive the substrate and the process gas. The system further includes an interior surface contiguous with the reaction chamber. A buffer gas supply system is adapted to supply a flow of a buffer gas between the interior surface and at least a portion of the process gas such that the flow of the buffer gas forms a gas barrier layer to inhibit contact between the interior surface and components of the process gas when the process gas is disposed in the reaction chamber.



101
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180A
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172
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EXHAUST GAS
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100A
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Fig. 1

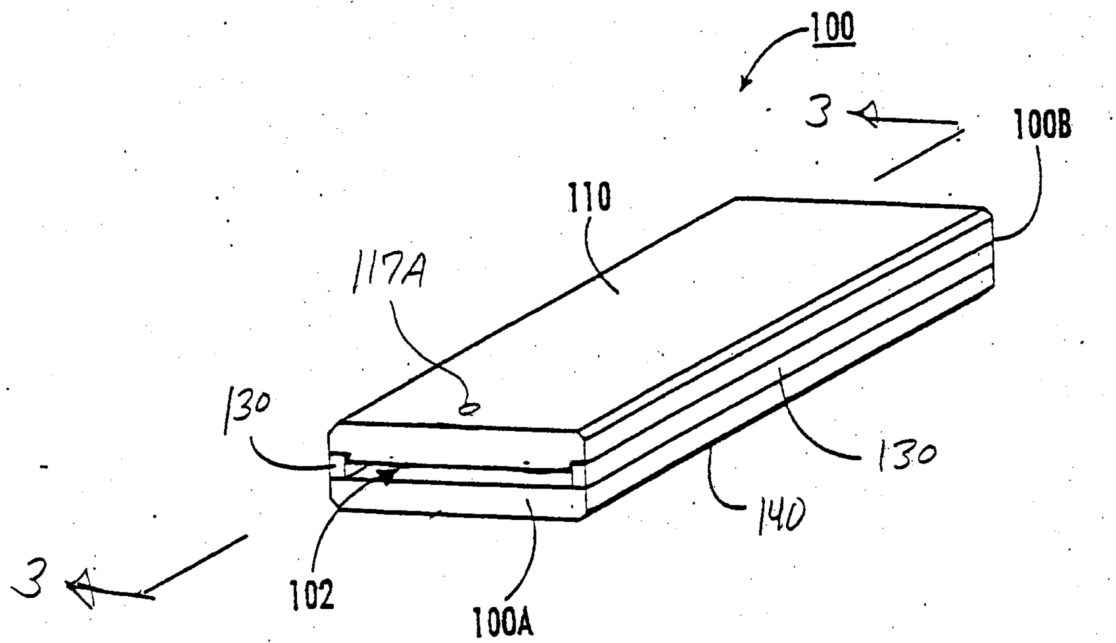

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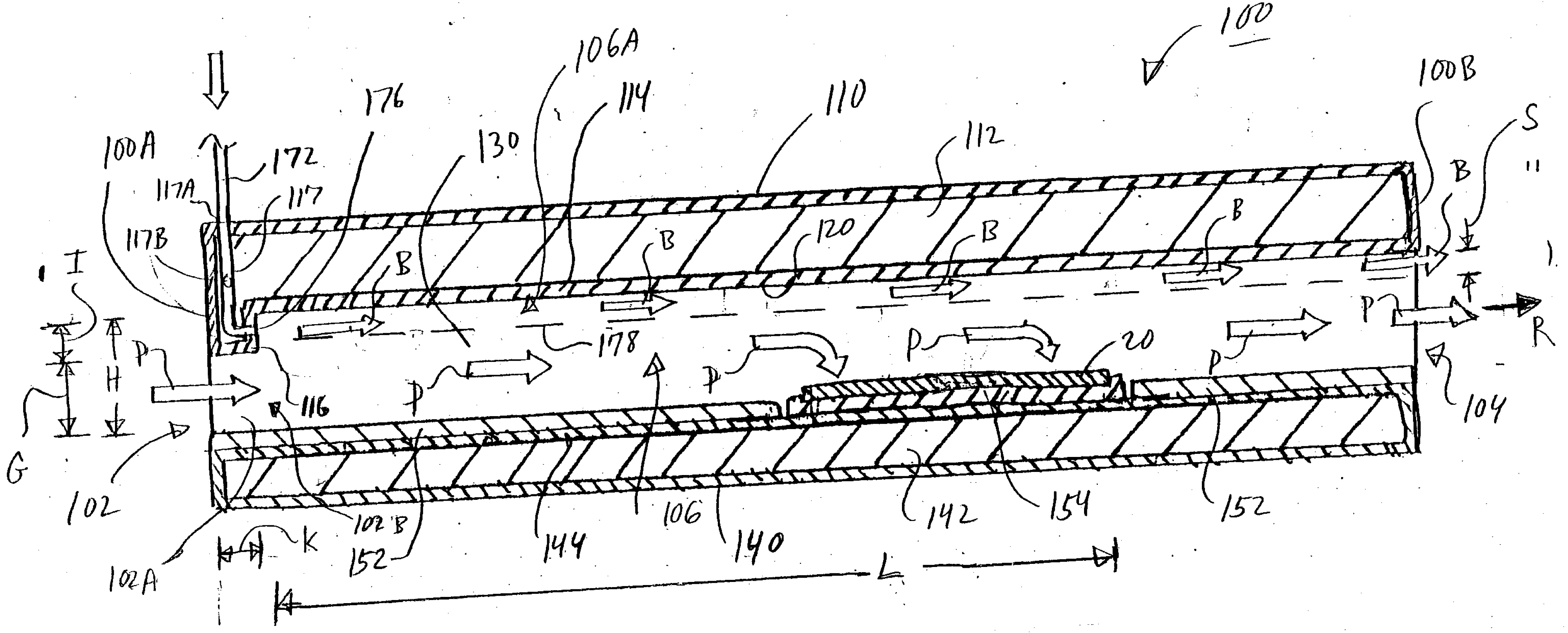
Fig. 2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154
102A
K
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Fig. 3

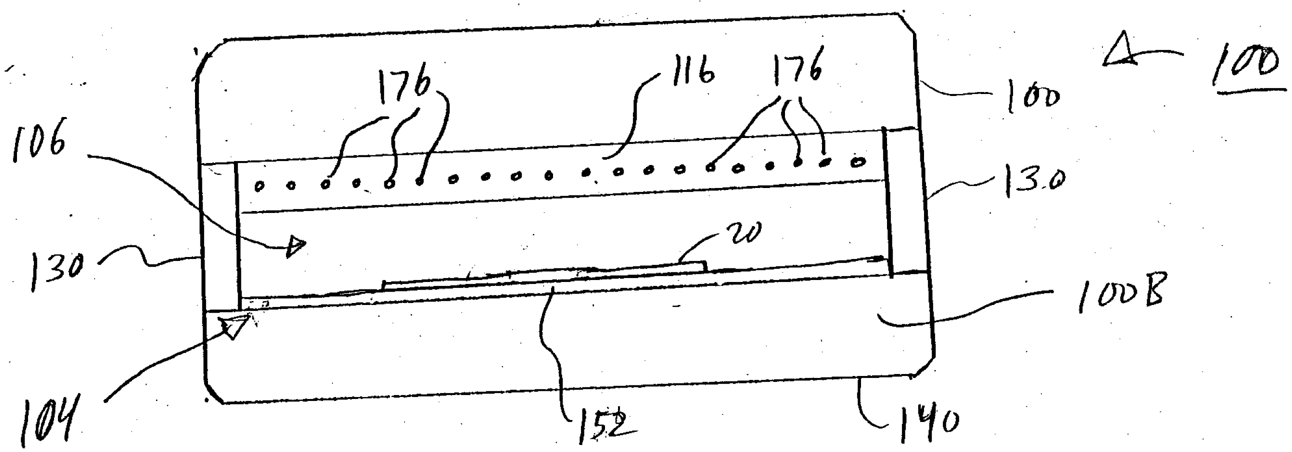
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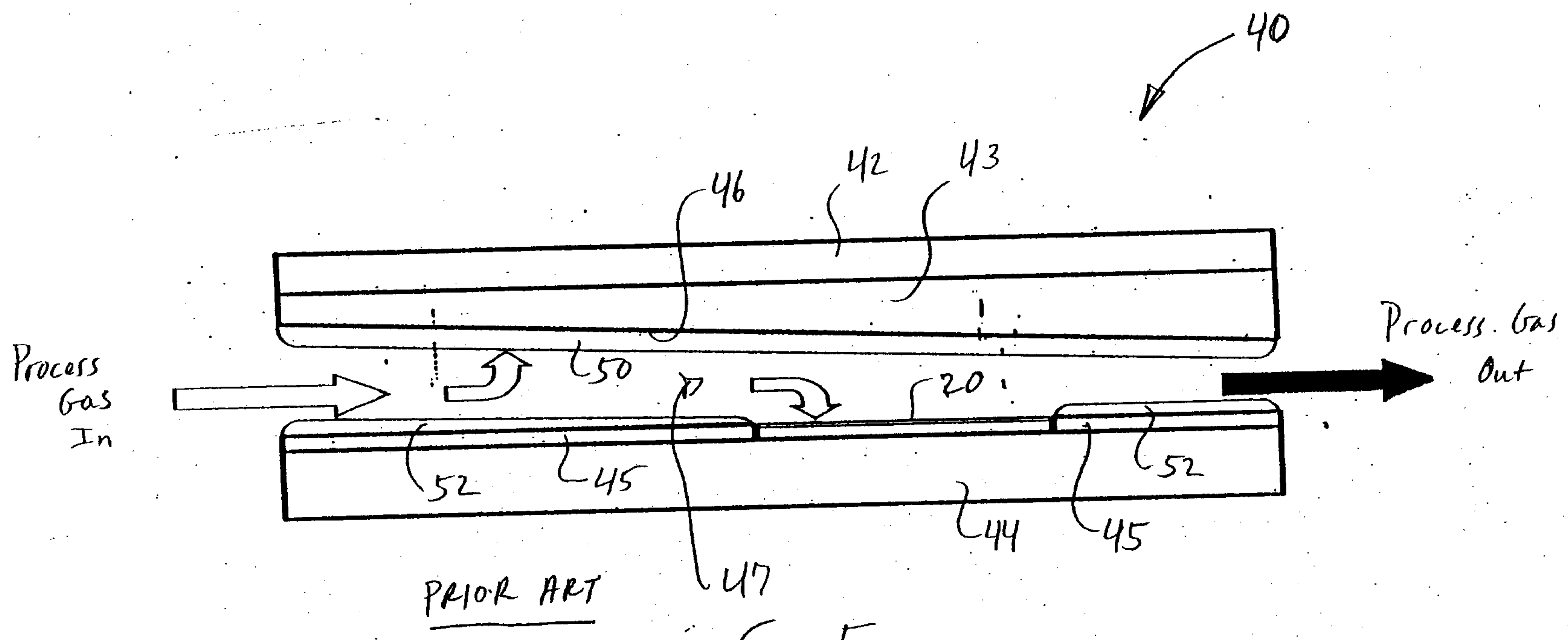
Fig. 4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Process Gas In
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Process Gas Out
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52
PRIOR ART

Fig. 5

METHOD TO REDUCE STACKING FAULT NUCLEATION SITES AND REDUCE V_F DRIFT IN BIPOLAR DEVICES

FEDERAL RESEARCH STATEMENT

[0001] This invention was developed under government contract No. N00014-02-C-0302. The U.S. Government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms as provided for by the terms of contract No. N00014-02-C-0302 awarded by the Defense Advanced Research Projects Agency ("DARPA").

RELATED APPLICATIONS

[0002] This is a continuation-in-part of Serial No. 10/605,312 filed September 22, 2003 and now U.S. Patent No. ___________.

BACKGROUND

[0003] The present invention relates to increasing the quality and desired properties of semiconductor materials used in electronic devices, particularly power electronic devices. In particular, the invention relates to an improved process for minimizing crystal defects in silicon carbide, and the resulting improved structures and devices. The present invention is related to the subject matter disclosed and claimed in commonly assigned U.S. Patent No. 6,849,874; the contents of which are incorporated entirely herein by reference.

[0004] Silicon Carbide

[0005] Silicon carbide (SiC) has emerged over the last two decades as an appropriate candidate semiconductor material that offers a number of advantages over both silicon and gallium arsenide. In particular, silicon carbide has a wide bandgap, a high breakdown electric field, a high thermal conductivity, a high saturated electron drift velocity, and is physically extremely robust. In particular, silicon carbide has an extremely high melting point and is one of the hardest known materials in the world.

[0006] Because of its physical properties, however, silicon carbide is also relatively difficult to produce. Because silicon carbide can grow in many polytypes, it is difficult to grow into large single crystals. The high temperatures required to grow silicon carbide also make control of impurity levels (including doping) relatively difficult, and likewise raise difficulties in the production of thin films (e.g. epitaxial layers). Because of its hardness, the traditional steps of slicing and polishing semiconductor wafers are more difficult with silicon carbide. Similarly, its resistance to chemical attack make it difficult to etch in conventional fashion.

[0007] In particular, silicon carbide can form over 150 polytypes, many of which are separated by relatively small thermodynamic differences. As a result, growing single crystal substrates and high quality epitaxial layers ("epilayers") in silicon carbide has been, and remains, a difficult task.

[0008] Nevertheless, based on a great deal of research and discovery in this particular field, including that carried out by the assignee of the present invention, a number of advances have been made in the growth of silicon carbide and its fabrication into useful devices. Accordingly, commercial devices are now available that incorporate silicon carbide to produce blue and green light emitting diodes, as a substrate for other useful semiconductors such as the Group III nitrides, for high-power radio frequency (RF) and microwave applications, and for other high-power, high-voltage applications.

[0009] As the success of silicon-carbide technology has increased the availability of certain SiC-based devices, particular aspects of those devices have become more apparent. In particular, it has been observed that the forward voltage (also referred to as "forward bias") of silicon carbide-based bipolar devices tends to increase noticeably during operation of those devices. For a number of reasons, such functional problems in semiconductor devices can often result from defects in the crystal structure of the material from which the devices are formed.

[0010] Crystallographic Defects

[0011] At the most basic level, structural crystallographic defects fall into four categories: point defects, line defects, planar defects and three dimensional defects. Point defects include vacancies, line defects include dislocations, planar defects include stacking faults and three-dimensional defects include polytype inclusions.

[0012] A dislocation is a kind of structural imperfection that extends for many unit cell lengths throughout a crystal. A more definite description of dislocation classifies them as screw and edge dislocations. As recognized by those persons skilled in this art, a symmetrical path followed from atom to atom (or from ion to ion) in a real crystal that returns upon itself, it is referred to as a Burgers circuit. If the same path in the lattice that typifies the structure does not return upon itself, so that the beginning and end do not lie on the same atom, then the Burgers circuit encloses one or more dislocations. The vector that completes the closed circuit in the lattice is referred to as the Burgers vector and measures the magnitude and direction of the dislocation.

[0013] If the Burgers vector is parallel to the line that locates the dislocation, the defect is referred to as a screw dislocation. Alternatively, if the Burgers vector is perpendicular to the dislocation, it is referred to as an edge dislocation. The simplest version of an edge dislocation is an incomplete plane of atoms or ions interleaved between two normal planes in a manner somewhat analogous to an extra card inserted halfway into a deck. On one side of the dislocation line, the planes separate to make room for the extra layer; on the other side the planes compress due to the absent layer.

[0014] Screw dislocations are not necessarily disadvantageous and, in fact, can be particularly important for the growth of a crystal face. A screw dislocation always presents one edge that is one or a few atoms high. At this edge, continued growth of the crystal is relatively easy. Dislocations, however, allow plastic flow to occur in a crystal relatively easily. In a limited region, the dislocation line created by the dislocation may be almost a straight line. Any plane that contains the Burgers vector and a segment of the dislocation line is referred to as a "slipped plane". The edge dislocation moves relatively easily through the crystal because motion in the slipped plane involves only a slight displacement of the structural elements. Stated differently, the slipped planes provide a low-energy intermediate state by which a crystal can be reorganized.

[0015] Defects in Silicon Carbide

[0016] In silicon carbide power devices, the availability of such relatively low-energy intermediate state encourages faults to continue to grow as the operation of the device provides the relatively small amount of energy necessary for the crystal reorganization.

[0017] Commercial quality SiC wafers and epilayers include both screw and edge dislocations. These dislocations can be further grouped by their alignment within the crystal.

Those dislocations that propagate along the c-axis are called threading dislocations, while dislocations that lie within the c-plane are termed basal plane dislocations. In general, in SiC, it is energetically favorable that basal plane dislocations preferentially decompose into partial dislocations via the mechanism described below:

$$1/3\langle 11\bar{2}0\rangle \rightarrow 1/3\langle 10\bar{1}0\rangle + 1/3\langle 01\bar{1}0\rangle \qquad \text{Equation 1}$$

[0018] The above decomposition reaction describes the decomposition of a basal plane dislocation into two Shockley partial dislocations. The line defects generated during the above decomposition will bound a planar stacking fault defect. In fact, partial dislocations will bind the entire perimeter of the stacking fault unless the stacking fault reaches a free surface. This stacking fault will be electrically active in bipolar devices and during forward operation, the electron-hole plasma will be reduced in the vicinity of the stacking fault. The reduced plasma density will increase the forward voltage (V_f) of the device. A further complication is that through dislocation enhanced dislocation glide, the stacking fault may continue to expand during forward operation of the device. This behavior is a substantial barrier to device exploitation because it results in devices with functional properties that can change unpredictably during operation.

[0019] Stated differently, the application of electric current through a silicon carbide bipolar device tends to initiate or propagate (or both) changes in the crystal structure. As noted above, many SiC polytypes are in close thermodynamic proximity, and solid phase transformations are quite possible. When the stacking faults progress too extensively, they tend to cause the forward voltage to increase in an undesirable manner that can prevent the device from operating as precisely as required or desired in many applications.

[0020] In some conventions, dislocation density is described by centimeters of dislocation length per cubic centimeter of material, and thus report dislocation density units of per square centimeter (cm^{-2}). In another convention (and as used herein) the off-axis orientation of 4H-SiC substrates for SiC epilayer growth and the common etch technique used to detect dislocations make it more convenient to use etch pit density (also in the units of cm^{-2}), to describe dislocation densities in SiC. Those of skill in this art will thus recognize that for a given dislocation density expressed as cm/cm^3, one could get a very different dislocation pit density when expressed as pits/cm^2 depending on the typical dislocation configuration and the off-axis angle of the substrate. Therefore, although the two numbers will have the same net units (cm^{-2}), they do not necessarily indicate the same actual dislocation density. For the sake of clarity and consistency, in this disclosure, dislocation density will only be described as the density of specific pits delineated on an etched epi-surface of a silicon face prepared, 8° off-axis (0001) oriented substrate.

[0021] Present commercially available 4H-SiC substrates have approximately 1E3 to 1E5 (10^3-10^5) dislocations per cm^2 by the convention used herein. This includes threading screw and edge dislocations, micropipes and basal plane dislocations. Figure 1 is a micrograph of KOH-etched epilayer surface revealing various common types of dislocation pits (the exact nature of which are set forth in the Detailed Description). All types of dislocations can impact device performance, but the basal plane dislocation is particularly implicated as being the prevalent nucleation site of the stacking faults that cause V_f drift.

[0022] In turn, defects in the substrate are often replicated in epitaxial layers grown on such substrates, thus making substrate crystal quality an important factor with respect to the quality and performance of resulting devices.

[0023] Conventional substrate preparation and epilayer growth practices will fairly effectively reduce the density of basal plane dislocations from 1E3- 1E4 cm^{-2} in the substrate to about 400 cm^{-2} in the epilayer. This reduction in dislocation density is accomplished via changes in both the substrate preparation and the epilayer growth operations.

[0024] Because SiC is a very hard material, preparing a typical substrate requires fairly aggressive sawing, lapping and polishing operations. These steps all generate sub-surface damage including enormous numbers of dislocations, including basal plane dislocations. To remove this damaged region, in practice, a less aggressive final preparation, such as chemical mechanical polishing (CMP) or a dry etch is employed after wafer shaping to remove sub-surface damage. The inventors herein have observed, however, that in many cases sub-surface damage propagates several microns beyond the depth removed by such conventional final surface preparation. In particular, and without wishing to be bound by any particular theory, it is hypothesized (but not yet confirmed) that damage from the sawing operation is the predominant cause of the residual damage.

[0025] Accordingly, continued improvement in the structure and operation of SiC-based bipolar devices will require continued improvements in the underlying substrates and their crystal structures.

Summary of the Invention

[0026] The invention is a method of preparing a substrate for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices. The method includes the steps of conducting a first non-selective etch on the surface of a silicon carbide substrate to remove both surface and subsurface damage; thereafter conducting a selective etch on the same surface sufficient to delineate the intersection of basal plane dislocations with the wafer surface and that will thereafter tend to propagate into epilayers as threading defects while avoiding creating beta (3C) inclusions and carrot defects; growing an epitaxial layer on the selectively etched substrate surface to a thickness greater than that of the typical threading etch pit depth in the selectively-etched surface to thereby provide the epitaxial layer with a sufficient thickness to support additional polishing and etching steps above the substrate; polishing away a sufficient portion of the epitaxial layer to remove the material containing the etched pits to thereby provide a surface with fewer etched pits than the surface of the selectively-etched substrate; and conducting a second non-selective etch of the epilayer sufficient to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer.

[0027] The foregoing and other objects and advantages of the invention and the manner in which the same are accomplished will become clearer based on the followed detailed description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

[0028] Figure 1 is a photograph of the surface of a SiC substrate following an etch in molten KOH.

[0029] Figure 2 is a photograph of a carrot defect on a SiC surface.

[0030] Figure 3 is a photograph of the same carrot defect following an etch in molten KOH.

[0031] Figure 4 is a photograph of a SiC surface that has been etched from Si droplets that formed during epilayer growth.

[0032] Figure 5 is a schematic diagram of the influence of a KOH etch on the propagation of basal plane defects.

[0033] Figure 6 is a plot of basal plane dislocation density versus surface preparation technique.

Detailed Description

[0034] The invention is a method of preparing a substrate for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices.

[0035] In a first embodiment the method initially comprises conducting a non-selective etch, preferably a dry etch, most preferably a reactive ion etch (RIE), on the surface of a silicon carbide substrate to remove both surface and subsurface damage that typically results from the sawing and lapping of the extremely hard SiC material. As known to those familiar with the manufacture of electronic devices, a nonselective etch removes all material at an equal rate. A selective etch removes specific materials—e.g. damaged, n-type, p-type—more quickly than the other materials. Exemplary, but not limiting, techniques for dry etching of silicon carbide are set forth in U.S. Patents No. 4,865,685 and its sibling No. 4,981,551 the contents of which are incorporated entirely herein by reference. Other techniques and chemistries for carrying out the selective and non-selective etches described herein are generally well-recognized in the art and will not be described in detail herein other than to illustrate embodiments of the invention.

[0036] The term "substrate" is used herein in a sense that is broad enough to include both a bulk single crystal (usually cut from a boule) as well as a device precursor structure that can include one or more epitaxial layers, but which fundamentally (although not necessarily exclusively) serves as the physical and electronic support for a device formed thereon.

[0037] Similarly, the terms "dry etch" and "wet etch," are often used to refer to reactive ion or plasma etches ("dry") or to etches in molten salts or other solutions ("wet").

[0038] In a preferred embodiment, the initial non-selective etch is carried out to a depth of approximately five microns. A standard etch, by way of comparison, only removes about one micron of material, because a more extensive RIE etch may tend to create a large number of auto-masking defects and pits on the wafer.

[0039] Following the nonselective etch, the method comprises conducting a selective etch on the same surface sufficient to reveal the etch pits of basal plane dislocations while avoiding creating beta (i.e., the 3C polytype) inclusions and carrot defects in subsequent epilayer growth. In preferred embodiments the selective etch is carried out with a molten salt, with molten potassium hydroxide ($KOH_{(l)}$) being one such preferred salt. The nature of molten salt etches is generally well understood by those of skill in this art and will not otherwise be described in detail. In somewhat simplistic terms, the selective etch is the functional opposite of crystal growth; i.e., in the same manner that a crystal tends to grow differently at different structural features, the etch will tend to remove material differently at different structural features, and thus highlight them.

[0040] The potassium hydroxide etch is typically carried out for between about 20 and 45 minutes at a temperature of about 450° Centigrade. In establishing the time and temperature, an insufficient KOH etch will not sufficiently reveal basal plane dislocations. Alternatively, an excessive KOH etching will create 3C (beta) polytype inclusions and carrot defects during subsequent epilayer growth on the etched surface. In most cases, the temperature of about 450°C keeps the etch appropriately selective. A higher temperature etch tends to become non-selective and produce an undesired set of resulting broader pits. For example, 600°C appears to be too high as one empirical upper limit, while the melting point of the etchant represents the functional lower limit.

[0041] Performing a mild KOH etch of the substrate after the extended dry etch tends to further reduce the basal plane dislocation density in epilayers that are later grown on the substrate. This improvement is attributed to the different growth mechanism over the morphology (etch pit) in the immediate region where the basal plane dislocation intersects the substrate surface. The KOH etch delineates the basal plane immediately down-step from the dislocation. As epilayer growth progresses on this surface, there is an enhanced opportunity for the basal plane dislocation to reorient to a threading dislocation and thereby reduce the total dislocation length and also reduce the free energy of the crystal.

[0042] Stated differently, the selective etch helps create a morphology that encourages dislocations that have originated as basal plane dislocations to either terminate or to thereafter propagate (into epilayers) as threading dislocations. In turn, the threading dislocations tend to remain unaffected (or at least much less affected) by forward voltage during operation of resulting devices.

[0043] The selective etch can also be carried out using a eutectic, or near eutectic, etchant; e.g. of molten KOH and sodium hydroxide (NaOH)

[0044] Controlling two main factors encourages a consistent etch: etch rate and selectivity. The etch rate is normally expressed in terms such as microns etched per hour. In general, etch rate increases as etchant temperature increases.

[0045] Selectivity describes how local variations in the sample being etched impacts the local etch rate. As used herein, selectivity refers to the ratio of the etch rate on the carbon face of a wafer to the etch rate on the silicon face of the wafer. A similar selectivity, in response to variations in local crystal strain, is exhibited on a particular face by the extent to which a distinct etch pit forms at the intersection of a dislocation with the sample surface. For basal plane dislocation conversion, the shape and size of the etch pit plays a significant role in the efficacy of the conversion. As is typical with chemical etchants, the selectivity decreases with increasing etch temperature.

[0046] For a selective etch used as a prelude to the conversion of basal plane dislocations, a low etch rate favors repeatability. Because a slower etch rate requires a longer etch time, any inadvertent variations in the etch time have a proportionally reduced impact. Molten KOH etching is not as easily performed as most wet etches, and the immersion and removal steps are cumbersome and hard to standardize. This favors using a lower etch temperature.

[0047] The desire for selectivity also favors using a lower etch temperature. In practice, an etch temperature of between about 400 and 450 °C works as a good compromise. Lower temperatures unfavorably approach the freezing point of KOH (about 360 °C) while higher temperatures (as noted above) lower the resulting selectivity. Additionally as the etchant is used and becomes more contaminated, the freezing point seems to gradually increase. As a result, the etch begins to approach the lower temperature limit, and when the relatively cool wafers are immersed, some KOH will tend to freeze onto the wafer and create odd etch artifacts.

[0048] The eutectic etch of KOH and NaOH behaves (etch rate and selectivity) about the same as pure KOH at a given temperatures. As a benefit, however, the eutectic etch has a melting (freezing) point of about 170 °C; i.e., within a much more stable realm.

[0049] Although by formal definition, the eutectic of KOH and NaOH is the proportional combination with the lowest melting point, in practice the actual etchant composition can differ, either inadvertently or deliberately, for a number of reasons. For example if one component of the solution is preferentially depleted, the initial composition may be offset from the exact eutectic.

[0050] Following the nonselective and selective etches, the method next comprises growing a semi-sacrificial epitaxial layer, preferably (but not necessarily) of n-type conductivity, on the selectively etched substrate surface to a thickness much greater (e.g. at least about 50 percent greater) than that of the typical threading dislocation etch pit depth (which are generally deeper than basal etch pits) in the selectively-etched surface to thereby provide the epitaxial layer with a sufficient thickness to support additional polishing and etching steps above the substrate. Once the semi-sacrificial layer is sufficient to support the following steps, additional thickness offers no extra advantage, and an overly-thick layer adds nothing other than the need to remove additional material for its own sake. In preferred embodiments, the semi-sacrificial epilayer is about 30-50 microns (μ) thick to provide at least about 15 μ for polishing removal, about 5 μ for additional RIE removal (these steps are described immediately below) and about 10 μ of improved material remaining as the desired epilayer surface.

[0051] Generally--but not necessarily--the substrate will be n-type, because n-type substrates offer a number of advantages in silicon carbide-based devices, and will have an activated carrier concentration of about 1E18-1E19 ($1 \times 10^{18} - 1 \times 10^{19}$ carriers per cm^3). In comparison to the substrate, the carrier concentration of the epitaxial layer is selected (or described) in terms of its purpose. "Conductive" layers will typically have a carrier concentration of 1E18-19. "Blocking" layers will typically have carrier concentrations less than 1E16. “Active” layers will have carrier concentrations within these parameters, depending on the structure or purpose of the end device. Accordingly, although terms such as n, n+ and n- can be used to describe both substrates and epilayers, such terminology should be considered in an illustrative rather than a limiting sense.

[0052] In a next step, the method of the invention comprises polishing away a sufficient portion of the semi-sacrificial epitaxial layer, typically about 15 μ, to remove the material containing the etched pits to thereby provide a surface with fewer pits than the surface of the original substrate. In preferred embodiments, the polishing can be carried out chemically or mechanically or both, with such steps being generally well-understood in this art.

[0053] In a final preparation step, the method of the invention thereafter comprises conducting a second non-selective etch (with RIE being typically preferred) of the semi-sacrificial epilayer sufficient to remove subsurface damage from the polishing step, but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate. In a preferred embodiment, the second non-selective etch is used to remove about 5 more microns from the semi-sacrificial layer.

[0054] Because the method of the invention provides a superior surface for epilayer growth, the method can further comprise forming a bipolar device by forming a n-type epitaxial layer above the polished and etched surface of the epitaxial layer, and forming a p-type epitaxial layer above the polished and etched surface of the epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers. As used herein, the phrase “above” a layer can include forming one layer immediately upon another layer, or on one or more intermediate layers provided that the intermediate layers do not otherwise interfere with the layers of interest. Such intermediate layers may be included for various structural or functional purposes, including providing appropriate buffers and transition layers in a device or device precursor that do not otherwise affect the basic design of the desired bipolar device. In this manner, the invention can be advantageously incorporated into any semiconductor device that experiences V_f drift or performance degradation similar to V_f drift such as recombination enhanced dislocation glide.

[0055] In preferred embodiments, preparing a bipolar device includes the steps of etching the n-type silicon carbide substrate, growing, polishing and etching the semi-sacrificial n+ epitaxial layer on the selectively etched substrate surface, growing an n-type epitaxial layer above the polished and etched n+ epitaxial layer, and growing a p-type epitaxial layer above the n-type epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers.

[0056] The silicon carbide substrate upon which the device is formed can be taken from a larger crystal (or "boule"), typically by the steps of sawing a silicon carbide substrate wafer from a silicon carbide boule, and thereafter conducting the nonselective etch on the substrate wafer. In most circumstances, the sawed substrate wafer is lapped, polished, etched (typically RIE), and cleaned (with an acid or solvent) prior to conducting the first isotropic (nonselective) etch of the method of the invention. The term "lapped" is used in its typical sense; i.e., to describe the steps of flattening the wafer surfaces using a counter-rotating lapping machine and an abrasive (e.g. diamond) slurry. Lapping helps make the wafer surfaces parallel and reduces mechanical defects such as saw markings. Similarly, the polishing etching and cleaning steps are otherwise carried out conventionally prior to the steps of the present invention.

[0057] The invention advantageously reduces the density of basal plane dislocations in the epilayer by a factor of at least two orders of magnitude as compared to more conventional techniques. This reduction in basal plane dislocation density along with the measures identified to isolate active device regions from the substrate and surface defects discussed in previously-incorporated Patent No. 6,849,874 represent a major step to commercializing SiC bipolar devices.

[0058] Additional aspects of the invention can be understood with respect to the drawings.

[0059] Figure 1 is a micrograph of the surface of a silicon carbide epitaxial layer etched with potassium hydroxide (KOH) and revealing various common types of dislocation pits. As set forth elsewhere herein, many types of dislocations can impact device performance, but the basal plane dislocations are particularly implicated as being the prevalent nucleation site of the stacking faults that cause the undesired drift under forward bias. In Figure 1, several (but not necessarily all) of the basal plane dislocation etch pits are designated at 10. A micropipe is designated at 11, a threading screw dislocation at 12, and threading edge dislocations at 13.

The basal plane dislocation etch pits are in part identified by having a generally oval shape with one frequently faceted edge, with the deepest part of the pit being visible nearest to the faceted edge. The micropipe 11 is identified by its generally larger size and its hexagonal geometry characteristic of the crystal packing structure of silicon carbide. The threading screw dislocations are identified with the deepest portion being at or near the center of the pit. Because the photographed surface has an 8° off-axis orientation with respect to the basal plane, the etch pit bottoms in Figure 1 appear slightly off-center.

[0060] Figure 2 illustrates a carrot defect 14 (identified by its characteristic shape, from which it derives its name) on the surface of the silicon carbide epitaxial layer. Figure 3 is a photograph of the surface of Figure 2, following the potassium hydroxide etch and showing the manner in which the etch delineates the carrot defect along with the basal plane dislocations, the threading screws and the threading edge dislocations.

[0061] Figure 3 illustrates the same surface as Figure 2, but after a KOH etch of the type used and described herein has developed pits corresponding to the carrot defect, as well as to basal plane and threading screw and threading edge dislocations.

[0062] Figure 4 illustrates a plurality of etched portions 15 on the surface of a silicon carbide epitaxial layer that form when silicon droplets etch the silicon carbide surface during epitaxial layer growth.

[0063] Figure 5 schematically illustrates the manner in which the selective etch can favorably influence the propagation of basal plane defects into threading dislocations. In Figure 5, the surface of a substrate 19 is designated at 20 and a basal plane is designated at 21, and is off axis (8° in preferred embodiments) from the substrate surface 20 for other favorable growth purposes. Individual layers of atoms in the crystal are designated at 23. During epitaxial growth, "adatoms" (those atoms from the source gases that form the growing crystal) represented by the arrows 24 diffuse across the substrate surface 20 and add to the available sites on the crystal surface. Because the crystal is oriented 8 ° off-axis, atoms moving from right to left tend to add to the crystal more easily and frequently than those moving from left to right.

[0064] When the substrate 19 is etched and an etch pit (designated at 25) develops from a basal plane dislocation, the resulting morphology creates an even greater tendency for diffusing adatoms to add as they move from right to left and an even smaller tendency for them to add if moving from left to right. The resulting growth tends to favor a threading structure rather than a planar defect and such threading structures, as noted previously, appear to have little or no negative effect when a bias is applied to a resulting device.

[0065] Figure 6 presents some characteristic data from the basal plane dislocation reduction work, and plots basal plane dislocation density (as described earlier in pits-cm^{-2}) on a logarithmic Y-axis against the progressive preparation techniques for three-inch wafers along the X-axis. As set forth therein, a typical substrate includes about 10^3-10^5 cm^{-2} dislocations, following which growing an epitaxial layer reduces the density by about an order of magnitude (to about 10^2-10^3 cm^{-2}). Using either RIE or a molten KOH etch (but not both), the density can be reduced by about another order of magnitude (about 40-50 cm^{-2} in Figure 6), but neither RIE nor KOH shows a significant improvement over the other. Using the invention, however, the dislocation density can be reduced by yet another order of magnitude, i.e., to about 4-5 cm^{-2} for the data reported in Figure 6.

[0066] In order to take further advantage of the defect reduction in the substrate, the growth conditions for later (e.g. device) epilayers can be optimized to enhance the likelihood that the basal plane dislocations will become threading dislocations. Principally, this involves adjusting pre-etch, starting growth rate, and stoichiometry to generate a facile environment for dislocation turning.

[0067] Lastly, it is also possible to generate dislocation loops during epilayer growth. These loops can contain sections where the dislocation exhibits a basal character and these loop segments can decompose into Shockley partials and generate stacking faults. Epilayer growth conditions must be employed such that the loops do not form. In practice this means maintaining adequate surface mobility of adatoms (via sufficient temperature and stoichiometry) such that there is sufficient time to accommodate impinging material properly into the crystal before the additional depositing layers lock the previously deposited material in place.

[0068] The invention focuses on the behavior of a class of dislocations that historically have not been well addressed in SiC epilayer growth technology. The extended etches differ substantially from conventional practice. KOH etching or selectively etching the substrate prior to epilayer growth is very atypical. Ramping of growth rate is also unusual especially because doping and crystal quality control become problematic during the ramp. However these unusual steps offer the opportunity to dramatically reduce V_f drift as a technology limiting issue. The impact of these steps on device properties other than V_f drift remains to be evaluated.

[0069] The removal of damaged material by the extended dry etch can be accomplished by numerous other approaches. Sputtering, ion-milling, wet etching and CMP are some obvious alternatives. Further, refinements in the wafer shaping and polishing processes may reduce or eliminate the need for sub-surface damage removal.

[0070] The selective KOH etch may also be replaced by another etch technique or may be incorporated into final surface preparation steps or into an in-situ pre-epilayer growth treatment.

[0071] The approach can be of value for the production of any semiconductor device which experiences Vf drift or performance degradation similar to Vf drift such as recombination enhanced dislocation glide.

[0072] The techniques referred to herein are, taken individually, generally well-recognized and well-understood in the art and can be practiced without undue experimentation. Single crystal silicon carbide wafers of the type preferably used as starting structures herein are commercially available from Cree, Inc. 4600 Silicon Drive, Durham, North Carolina 27706. The growth of silicon carbide epitaxial layers can be carried out using techniques such as those set forth in U.S. Patents numbers 4,912,063; 4,912,064; 5,679,153; and 6,297,522. Dry and electrolytic etching of silicon carbide are described in U.S. Patents numbers 6,034,001; 5,571,374; 5,227,034; 4,981,551; and 4,865,685. The use of molten potassium hydroxide as an etchant to identify and characterize a semiconductor surface is well-understood, and includes versions expressed as ASTM standards (e.g. ASTM F1404.92). Cutting, mechanical polishing and lapping of substrate wafers are also entirely conventional in this art.

[0073] In the drawings and specification there has been set forth a preferred embodiment of the invention, and although specific terms have been employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being defined in the claims.

Claims

1. A method of preparing a substrate for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising:

conducting a selective etch on the surface of a silicon carbide substrate sufficient to delineate the basal plane dislocations with the wafer surface and that will thereafter tend to terminate or to propagate as threading defects while avoiding creating beta (3C) inclusions and carrot defects;

growing a conductive epitaxial layer on the selectively etched substrate surface to a thickness greater than that of the typical threading dislocation etch pit depth in the selectively-etched surface to thereby provide the epitaxial layer with a sufficient thickness to support additional polishing and etching steps above the substrate;

polishing away a sufficient portion of the conductive epitaxial layer to remove the material containing the etched pits to thereby provide a surface with fewer etched pits than the surface of the selectively-etched substrate; and

thereafter conducting a non-selective etch of the epilayer sufficient to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer.

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2. A substrate-preparation method according to Claim 1 comprising selectively etching the surface with a molten salt.

3. A substrate-preparation method according to Claim 2 comprising etching the surface with a molten salt selected from the group consisting of potassium hydroxide, mixtures of potassium hydroxide and sodium hydroxide, and a eutectic mixture of potassium hydroxide and sodium hydroxide.

4. A substrate-preparation method according to Claim 1 further comprising forming a bipolar device by:

forming a n-type epitaxial layer above the polished and etched surface of the epitaxial layer; and

forming a p-type epitaxial layer above the polished and etched surface of the epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers.

5. A device-preparation method according to Claim 4 comprising:

etching an n-type silicon carbide substrate;

growing, polishing and etching an n-type epitaxial layer on the selectively etched substrate surface;

growing another n-type epitaxial layer above the polished and etched epitaxial layer; and

growing a p-type epitaxial layer above the n-type epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers.

6. A method according to Claim 1 comprising growing a first device epitaxial layer immediately on the surface prepared by the non-selective etch.

7. A method according to Claim 1 comprising etching a single crystal silicon carbide ~~substrate having a polytype selected from the 3C, 4H, 6H and 15R polytypes of silicon~~ carbide.

8. A method of preparing a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising:

selectively etching the surface of a silicon carbide substrate to thereby develop etch-generated structures from at least any basal plane dislocations on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface; and thereafter growing a first epitaxial layer of silicon carbide on the selectively-etched surface.

9. A method according to Claim 8 comprising etching the surface with a molten salt as the selective etch.

10. A method according to Claim 9 comprising etching the surface with a molten salt selected from the group consisting of potassium hydroxide, mixtures of potassium hydroxide and sodium hydroxide, and a eutectic mixture of potassium hydroxide and sodium hydroxide.

11. A method according to Claim 8 comprising growing a conductive epitaxial layer on the selectively-etched surface.

12. A method according to Claim 10 comprising growing an n-type epitaxial layer on the selectively-etched surface.

13. A method according to Claim 8 comprising growing a second conductive epilayer above the first conductive epilayer and having the opposite conductivity type from the first conductive epilayer.

14. A method according to Claim 8 wherein the step of growing the first epitaxial ~~layer comprises forming a semi-sacrificial epitaxial layer on the selectively etched surface to~~ encourage the etched basal plane defects to reorient during subsequent growth into threaded defects;

and further comprising the steps of:

polishing the etched semi-sacrificial epitaxial layer to reduce etch pits; and

etching the polished semi-sacrificial epitaxial layer to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer;

all prior to forming the first epitaxial layer.

15. A method according to Claim 14 comprising forming the semi-sacrificial layer by chemical vapor deposition.

16. A method according to Claim 14 comprising polishing the etched semi-sacrificial epitaxial layer using a chemical-mechanical process.

17. A method according to Claim 14 comprising etching the polished semi-sacrificial epitaxial layer using a dry etch.

18. A method according to Claim 17 comprising etching the polished semi-sacrificial epitaxial layer using a reactive ion etch.

19. A method of preparing a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising:

selectively etching the surface of a silicon carbide substrate from which surface and subsurface damage have been removed to thereby develop etch-generated structures from at least any basal plane dislocations on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface; and thereafter

growing a first conductive epitaxial layer of silicon carbide on the selectively-etched surface.

20. A method according to Claim 19 comprising selectively etching the surface with a molten salt.

21. A substrate-preparation method according to Claim 20 comprising etching the surface with a molten salt selected from the group consisting of potassium hydroxide,

mixtures of potassium hydroxide and sodium hydroxide, and a eutectic mixture of potassium hydroxide and sodium hydroxide.

22. A method according to Claim 19 comprising growing a second conductive epilayer above the first conductive epilayer and having the opposite conductivity type from the first conductive epilayer.

METHOD TO REDUCE STACKING FAULT NUCLEATION SITES AND REDUCE V_F DRIFT IN BIPOLAR DEVICES

ABSTRACT

A method is disclosed for preparing a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices. The method includes the steps of etching the surface of a silicon carbide substrate with a nonselective etch to remove both surface and subsurface damage, thereafter etching the same surface with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocation reaching the substrate surface that will thereafter tend to either terminate or propagate as threading defects during subsequent epilayer growth on the substrate surface, and thereafter growing a first epitaxial layer of silicon carbide on the twice-etched surface.

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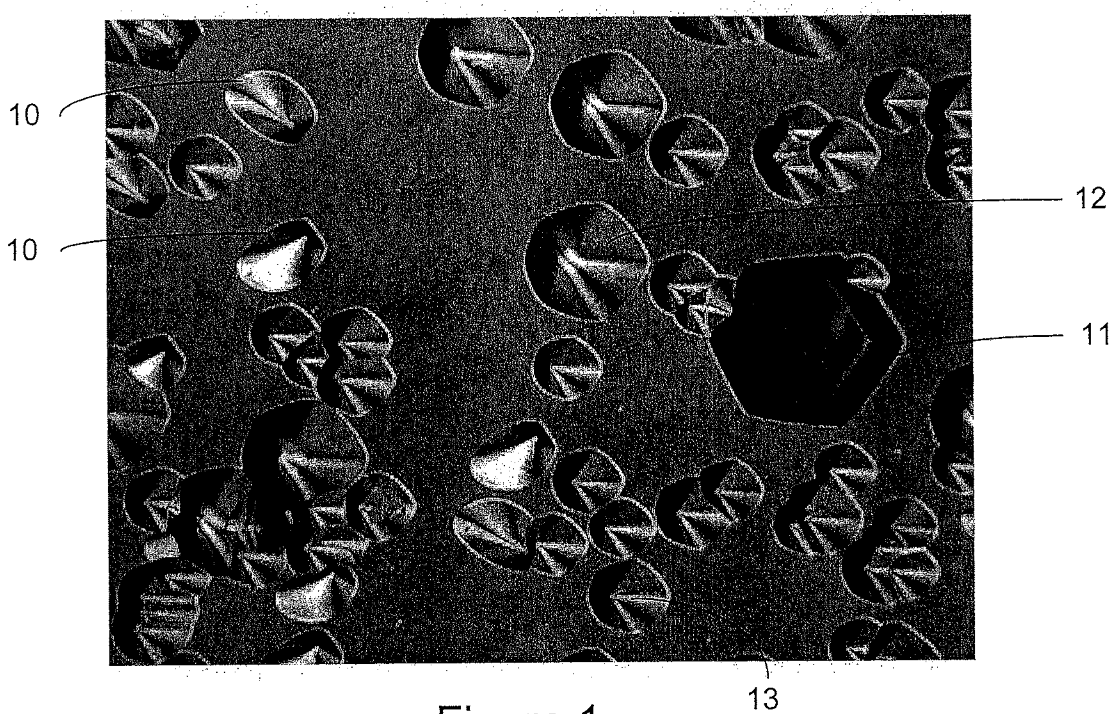

Figure 1

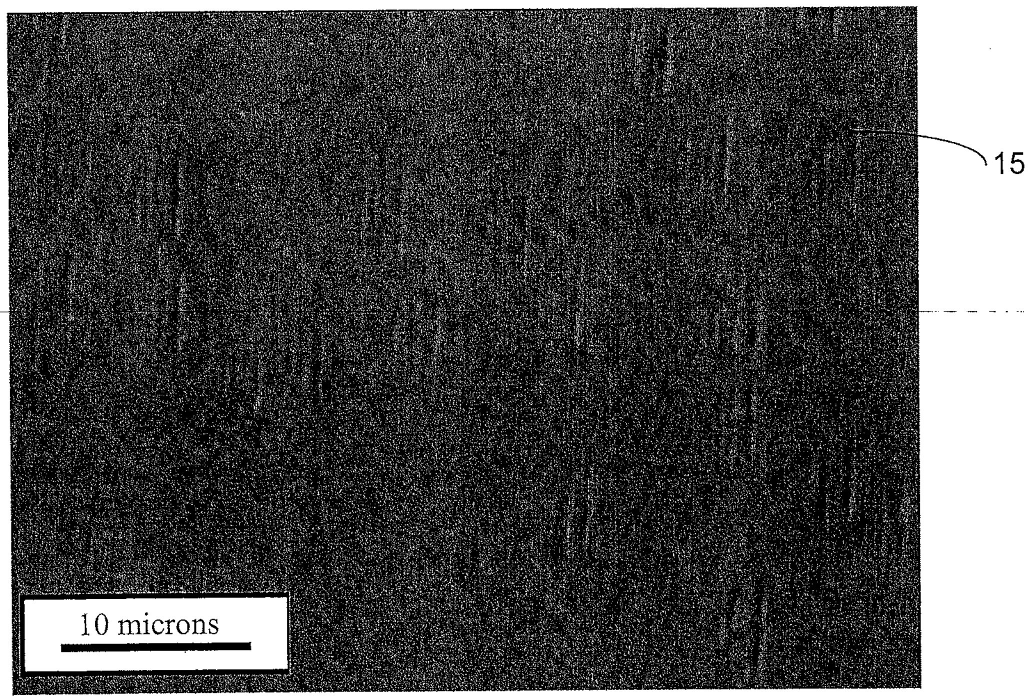

Figure 4

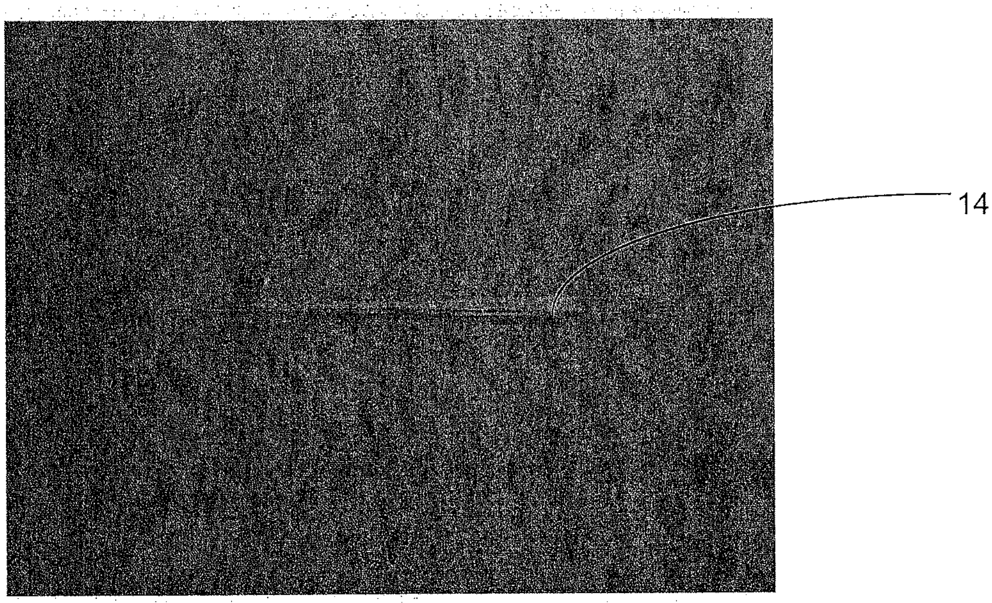

Figure 2

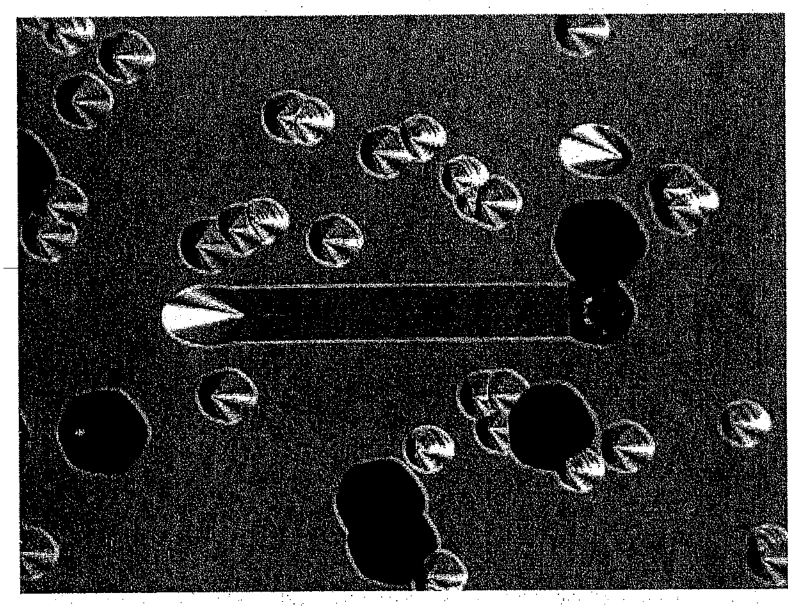

Figure 3

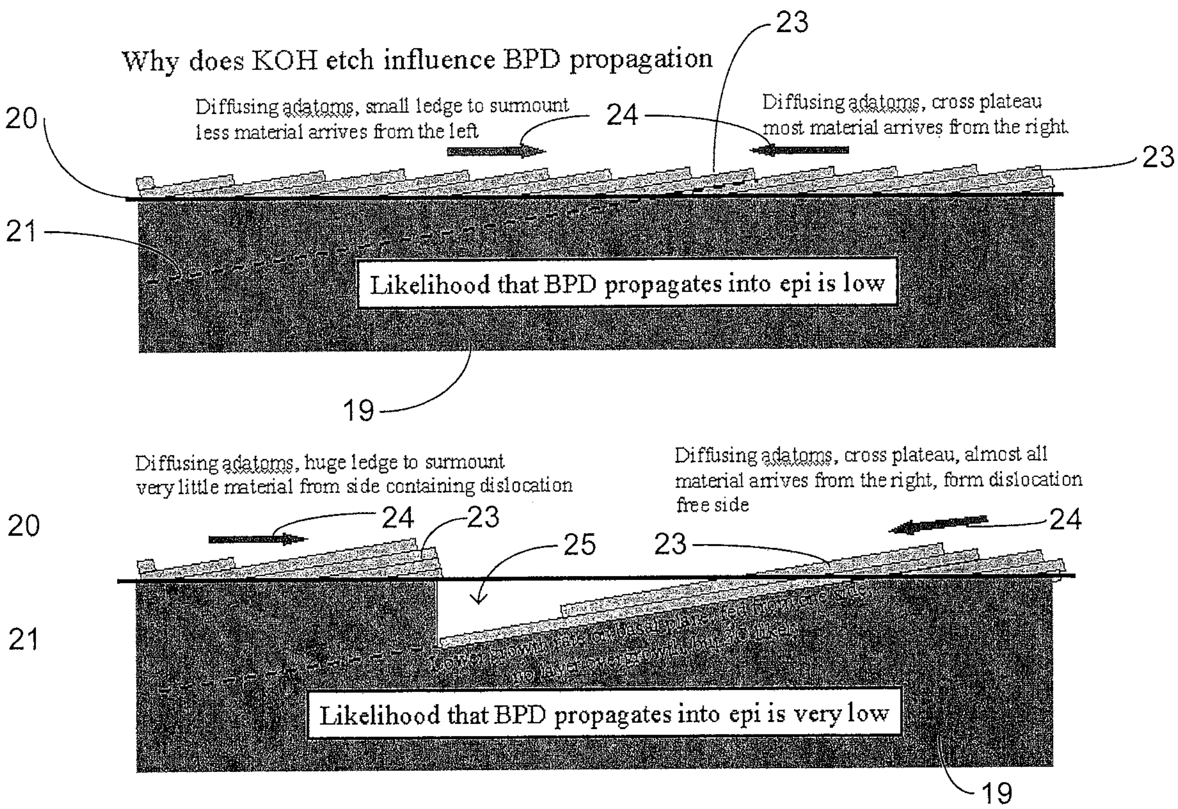

Figure 5

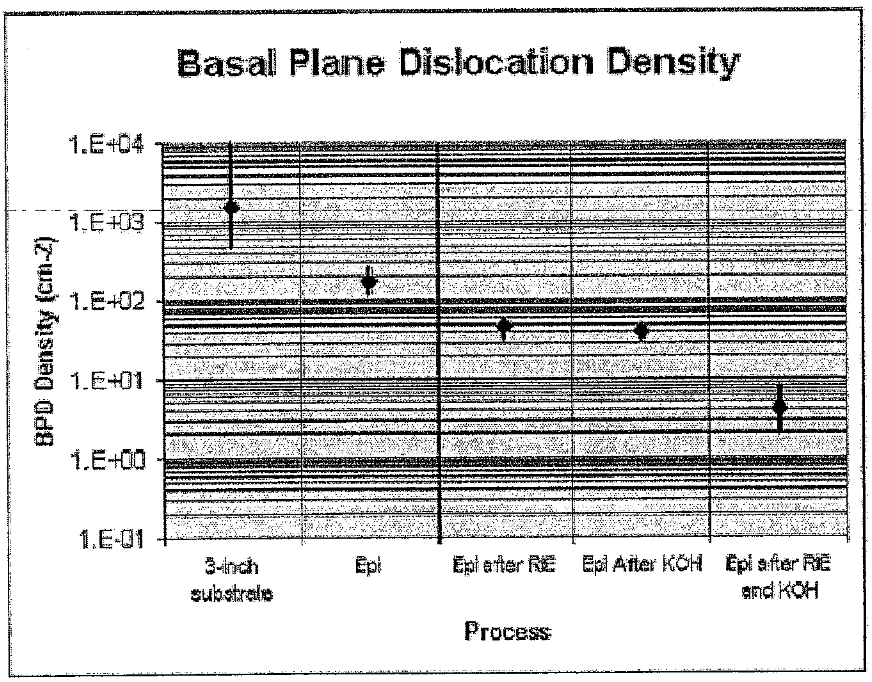

Figure 6

REDUCTION OF CARROT DEFECTS IN SILICON CARBIDE EPITAXY

Statement of Government Support

The present invention was made, at least in part, with government support under Office of Naval Research Contract No. N00014-02-C-0302. The United States government has certain rights to this invention.

Field of the Invention

The present invention relates to epitaxial deposition processes and, more particularly, to methods for depositing an epitaxial film of silicon carbide on a substrate and resulting epitaxial structures.

Background of the Invention

Deposition systems and methods are commonly used to form layers of semiconductor materials, such as thin epitaxial films, on substrates. For example, a chemical vapor deposition (CVD) reactor system and process may be used to form a layer of semiconductor material such as silicon carbide (SiC) on a substrate. CVD processes may be particularly effective for forming layers with controlled properties, thicknesses, and/or arrangements such as epitaxial layers. Typically, in a deposition system, such as a CVD system, the substrate is placed in a reaction chamber within a susceptor and one or more process gases including reagents or reactants to be deposited on the substrate are introduced into the chamber adjacent the substrate. The process gases may be flowed through the reaction chamber in order to provide a uniform or controlled concentration of the reagents or reactants to the substrate.

A deposition system, such as a CVD reactor, may be used to form epitaxial layers of silicon carbide on a single crystal silicon carbide substrate having a predetermined polytype such as 2H, 4H, 6H, 15R, 3C and the like. The term "polytype" refers to the ordering and arrangement of layers of atoms within a crystal structure. Thus, although the different polytypes of silicon carbide are stoichiometrically identical, they possess different crystal structures and consequently have different material properties such as carrier mobility and breakdown field strength. The letters H, R and C refer to the general crystal structure of the polytype, namely, hexagonal, rhombohedral and cubic, respectively. The numbers in the polytype designations refer to the repetition period of layer arrangements. Thus, a 4H crystal has a hexagonal crystal structure in which the arrangement of atoms in a crystal repeats every four bi-layers.

Figure 9 illustrates a hexagonal unit cell of a hypothetical crystal. The unit cell **60** includes a pair of opposing hexagonal faces **61A**, **61B**. The hexagonal faces are normal to the c-axis, which runs along the $\langle 0001 \rangle$ direction as defined by the Miller-Bravais indexing system for designating directions in a hexagonal crystal. Accordingly the hexagonal faces are sometimes called the c-faces which define the c-planes or basal planes of the crystal. Planes which are perpendicular to the c-plane are referred to as prismatic planes.

Silicon carbide possesses a number of advantageous physical and electronic characteristics for semiconductor performance and devices. These include a wide bandgap, high thermal conductivity, high saturated electron drift velocity, high electron mobility, superior mechanical strength, and radiation hardness. However, the presence of crystalline defects in silicon carbide films may limit the performance of electronic devices fabricated in the films, depending on the type, location, and density of the defects. Accordingly, significant research has focused on reducing defects in silicon carbide films. Certain defects, such as micropipes, are known to severely limit and even prevent device performance. Other defects, such as threading defects, are not considered to be electrically active, and therefore may not be detrimental to device performance, at densities normally found in epitaxial films.

For applications where a high voltage blocking capability is required (for example power switching applications), silicon carbide films are usually grown "off-axis." That is, the substrate crystal is sliced at an angle that is slightly oblique to the normal crystal axis (called the c-axis). Taking for example a hexagonal polytype such as 4H or 6H, the oblique angle of the cut may be made in one of the standard crystallographic directions illustrated in **Figure 10**, namely the $\langle 11\bar{2}0 \rangle$ direction (towards a point of the hexagonal unit cell) or $\langle 10\bar{1}0 \rangle$ direction (towards the center of a flat side of the hexagonal unit cell), or along a different direction.

Thus when an epitaxial layer is grown on the substrate, the deposited atoms bond to atoms at the exposed edges of the crystal layer steps, which causes the steps to grow laterally in so-called step-flow fashion. Step-flow growth is illustrated in

Figure 11. Each layer or step grows in the direction in which the crystal was originally cut off-axis (the $\langle 11\bar{2}0 \rangle$ direction in the case illustrated in **Figure 11**).

Surface morphological defects, i.e. defects in the shape of the surface of an epitaxial film, have been observed in silicon carbide epitaxial layers using conventional imaging techniques such as Transmission Electron Microscopy (TEM) and Nomarski microscopy. Surface morphological defects are generally considered to be caused by crystallographic defects in the material. Accordingly, research into the cause of surface morphological defects generally focuses on the physics of crystal growth.

Surface morphological defects are generally classified in accordance with their physical appearance. Thus, such defects have been classified as "comet", "carrot" and "triangular" defects based on their appearance under a microscope. Carrot defects are roughly carrot-shaped features in the surface of the silicon carbide film. The features are aligned along the step flow direction of the film, and are characteristically longer than the depth of the layer in which they are formed. For example, a film having a thickness of 40 μm may contain carrot defects having a length of around 250 μm depending on the off-axis angle. The mechanism by which carrot defects form is currently unknown. Wahab et al. speculate that carrot defects are caused by perfect screw dislocations which are pinned to the surface of the substrate during growth, and that the dislocation dissociates into partials that propagate in the basal plane and form partial ledges in the film. Wahab et al., "Influence of epitaxial growth and substrate induced defects on the breakdown of 4H-SiC Schottky diodes," Appl. Phys. Let. Vol. 76 no. 19, pp. 2725-2727 (2000). While Wahab et al. reported that carrot defects were not harmful to the absolute breakdown voltage of Schottky diodes, reverse leakage current was increased by the presence of carrot defects. Carrot defects may have deleterious effects on other device properties as well, particularly when the defect is located at a sensitive location, such as under the edge of a Schottky contact.

Thus, it would be desirable to reduce or minimize the concentration of carrot defects found in epitaxial films of silicon carbide.

Summary of the Invention

Some embodiments of the present invention, provide for manufacturing a single crystal silicon carbide epitaxial layer on an off-axis substrate by placing the substrate in an epitaxial growth reactor, growing a first layer of epitaxial silicon carbide on the substrate, interrupting the growth of the first layer of epitaxial silicon carbide, etching the first layer of epitaxial silicon carbide to reduce the thickness of the first layer, and growing a second layer of epitaxial silicon carbide on the first layer of epitaxial silicon carbide. Growing a first layer of epitaxial silicon carbide may include flowing silicon and carbon containing source gases over the substrate. Interrupting the growth of the first layer of epitaxial silicon carbide may include halting and/or reducing the flow of the source gases. Etching the first layer of epitaxial silicon carbide may include flowing an etchant gas such as H_2, HCl, Ar, Cl_2 and/or a carbon-containing gas such as propane over the substrate. Carrot defects which originate at the substrate/epitaxy interface may be terminated by the process of interrupting the epitaxial growth process, etching the grown layer and regrowing a second layer of epitaxial silicon carbide. The process of growth interruption/etching/growth may be repeated multiple times.

In certain embodiments of the present invention, a silicon carbide epitaxial layer having at least one carrot defect that is terminated within the epitaxial layer is provided.

Further embodiments of the invention provide a semiconductor structure that includes an off-axis silicon carbide substrate, an epitaxial layer of silicon carbide on the substrate, and a carrot defect having a nucleation point in the vicinity of an interface between the substrate and the epitaxial layer, wherein the carrot defect is terminated within the epitaxial layer.

Brief Description of the Drawings

Figure 1 is a schematic view of a deposition system according to some embodiments of the present invention;

Figure 2 is a cross section of a susceptor assembly forming a part of the deposition system of **Figure 1**;

Figure 3 is a plan view of a carrot defect in a silicon carbide epitaxial layer;

Figure 4 is a schematic side view of carrot defects formed in a silicon carbide epitaxial layer;

Figure 5 is a Nomarski micrograph of a pair of carrot defects in a silicon carbide epitaxial layer;

Figure 6 is a schematic side view of carrot defects formed in a silicon carbide epitaxial layer;

Figures 7(A)-(D) are micrographs of carrot defects in silicon carbide layers after KOH etching.

Figure 8 is a histogram showing the effects of embodiments of the invention;

Figure 9 is a schematic diagram of a hexagonal crystal unit cell structure;

Figure 10 is a top view of a hexagonal unit cell illustrating standard crystallographic directions; and

Figure 11 is a schematic side view of an off-axis silicon carbide crystal.

Detailed Description of the Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the relative sizes of regions or layers may be exaggerated for clarity. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Like numbers refer to like elements. As used herein the term "and/or" includes any and all combinations of one or more of the associated listed items.

It will be understood that although the terms first and second may be used herein to describe various elements, components, regions, layers, and/or sections, these elements, components, regions, layers, and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer, or section from another region, layer, or section. Thus, a first region, layer, or section discussed below could be termed a second region, layer, or section, and similarly, a second without departing from the teachings of the present invention.

A deposition system **101** in which embodiments of the present invention may be practiced is schematically shown in plan view in **Figure 1**. The deposition system **101** may be a horizontal, hot wall, flow through, CVD system as shown including a susceptor assembly **100**, a quartz tube **180** defining a through passage **180A**, an electromagnetic frequency (EMF) generator **182** (for example, including a power supply and an RF coil surrounding the tube **180**) and a process gas supply **160**. An insulative cover may be provided about the susceptor assembly **100** in addition to or in place of the quartz tube **180**. The deposition system **101** may be used to form a layer or film on a substrate **20** (**Figure 2**). While only a single substrate **20** is illustrated in **Figure 2**, the system **101** may be adapted to form films concurrently on multiple substrates **20**.

The substrate **20** may be a wafer or other structure formed of the same or a different material than that of the layer to be deposited. The substrate **20** may be formed of, for example, SiC, sapphire, a Group III nitride, silicon, germanium, and/or a III-V or II-VI compound or interalloy, or the like. The substrate surface upon which the film is deposited may be a base substrate or a first or subsequent layer superimposed on a base substrate. For example, the surface of the substrate **20** for receiving the deposited film may be a layer previously deposited using the deposition system **101** or an alternative apparatus. As will be appreciated by those of skill in the art in light of the present disclosure, embodiments of the present invention may be advantageously utilized with semiconductor materials other than those specifically mentioned herein.

Generally, the process gas supply **160** supplies a process gas into and through the susceptor assembly **100** as discussed below. The EMF generator **182** inductively heats the susceptor assembly **100** to provide a hot zone in the susceptor assembly **100** where deposition reactions take place. The process gas continues through and out of the susceptor assembly **100** as an exhaust gas that may include remaining components of the process gas as well as reaction by-products, for example. Embodiments of the present invention may be used in types of deposition systems other than hot wall CVD systems. Other modifications to the systems and methods of the present invention will be apparent to those of ordinary skill in the art upon reading the description herein.

The process gas includes one or more components such as reagents, reactants, species, carriers and the like. Where it is desired to form a SiC layer on a substrate, the process gas may include precursor gases such as silane (SiH_4) and propane (C_3H_8) along with a carrier gas such as purified hydrogen gas (H_2). The process gas supply

160 may be provided from one or more pressurized containers of the gases with flow control and/or metering devices as needed.

An exemplary conventional susceptor **100** is shown in **Figure 2**. The susceptor **100** may be used, for example, in a flow through, hot wall, CVD reactor. The susceptor **100** has a top susceptor member **100A** and a bottom susceptor member **100B**. The susceptor **100** also has a top liner **103** and a bottom liner **105** defining a reaction chamber **107** therebetween. A substrate **20**, such as a semiconductor wafer, is positioned in the reaction chamber **107** and may be situated on an interior surface of a platter (which may rotate), for example. A process gas **P** is introduced to the reaction chamber **107** at one end, flowed through the reaction chamber **107** past the substrate **20**, and finally exhausted from the reaction chamber **107** at the opposite end. As used herein, the term process gas refers to one or more gases. As indicated by the arrows in the reaction chamber **107** as shown in **Figure 2**, as the process gas flows through the reaction chamber **107** a portion of the process gas may contact the substrate **20** as intended and thereby deposit the reagents or reactants on the substrate **20** to form a layer thereon. In some systems, the reaction chamber **107** may have a length of between about 0.1 and 1 meter, a width of between about 0.05 and 0.5 meter, and a height of between about 1 and 10 cm. The reaction chamber **107** is not limited to these dimensions, however. The susceptor members may include high quality graphite. Examples of CVD deposition systems including improved susceptor designs are found in U.S. Patent Publication No. US 2003/0079689 entitled "*Induction Heating Devices and Methods for Controllably Heating an Article*" and U.S. Patent Application Ser. No. 10/414,787 entitled "*Methods and Apparatus for Controlling Formation of Deposits in a Deposition System and Depositions Systems and Methods Including the Same*" both of which are incorporated herein by reference in their entireties.

In certain embodiments, the susceptor members **100A, 100B** are formed of a material suitable to generate heat responsive to eddy currents generated therein by the EMF generator **182**, such materials and inductive heating arrangements being well known to those of skill in the art. The members may be formed of graphite, and more preferably of high purity graphite.

A platter **154** or the like may be situated between the bottom member **100B** and the substrate **20** to support the substrate **20**. According to some embodiments, the platter **154** may be rotatively driven by a suitable mechanism (not shown). For example, the system may include a gas-driven rotation system as described in Applicant's U.S. Application Serial No. 09/756,548, titled *Gas Driven Rotation Apparatus and Method for Forming Silicon Carbide Layers*, filed January 8, 2001, and/or as described in Applicant's U.S. Application Serial No. 10/117,858, titled *Gas Driven Planetary Rotation Apparatus and Methods for Forming Silicon Carbide Layers*, filed April 8, 2002, the disclosures of which are hereby incorporated herein by reference in their entireties. Alternatively, the platter **154** may be stationary. The platter **154** may be adapted to hold one or multiple substrates **20**. The platter **154** may be formed of any suitable material such as SiC coated graphite, solid SiC and/or solid SiC alloy. The platter **154** may be omitted such that the substrate rests on the bottom member **140**, the liner **105**, or other suitable support.

In use, the process gas supply **160** supplies a flow of the process gas **P** to the reaction chamber **107** through the inlet opening **102**. The process gas **P** flows generally in a flow direction **R**. As shown, some portion of the process gas and the reagents therein contact the substrate **20** to form the desired layer (e.g., an epilayer) on the exposed surface of the substrate **20**.

While the foregoing deposition system **101** and methods are described as relating to a horizontal, hot wall, CVD, flow through deposition process, various aspects of the present invention may be used in other types of deposition systems and processes. While particular embodiments have been described with reference to "top", "bottom" and the like, other orientations and configurations may be employed in accordance with the invention. For example, the deposition system and process may be a cold wall and/or non-horizontal flow through system and process. The deposition system and process may be a vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), or plasma enhanced CVD (PECVD) deposition system and process rather than a CVD system or process.

As discussed above, surface morphological defects known as carrot defects may form in silicon carbide epitaxial films. **Figure 3** is an optical image showing a carrot defect in a silicon carbide epitaxial layer. The defect appears as a carrot-shaped ridge in the surface of the material. Although the precise mechanism is unknown, it is presently believed that most, if not all, carrot defects form at the interface between the substrate and the epitaxial layers and then propagate through epitaxial growth. Okada et al. report that carrot defects are characterized by several sets of stacking faults on the (0001) plane at their termination, and observed partial dislocations bounding the stacking faults. Okada et al., "Crystallographic defects under surface morphological defects of 4H-SiC homoepitaxial films," ICSCRM 2003 Poster Session. The inventors have found that carrot defects tend to form at or near regions in which a high density of threading dislocations is present, such as may be present at the interface between a crystal substrate and an epitaxial layer. Carrot defects appear to propagate as stacking faults in prismatic planes which grow in stepwise fashion in the direction of the crystal off-cut. Viewed from the side, the defects appear as triangular stacking faults having a vertex at the substrate/epitaxy interface and an opposite side on the growth surface.

The formation of carrot defects is illustrated schematically in **Figure 4**, which shows a substrate **10** on which an epitaxial layer **20** has been formed. Carrot defects **A1** and **B1** are present in the epitaxial layer **20**. As the time scale adjacent the figure indicates, epitaxial growth of layer **20** is initiated at time t_0 and terminated at time t_2. Carrot defect **A1** nucleates at point **X** at the interface **12** and propagates upward as the epitaxial layer **20** grows. As illustrated in **Figure 4**, carrot defect **A1** is bounded on one side by a threading dislocation **31** in the $\langle 0001 \rangle$ direction and by a basal plane dislocation **32** aligned in the $\langle 11\bar{2}0 \rangle$ direction. When the epitaxial growth is terminated at time t_2, the carrot defect extends along the surface of the epitaxial layer **20** from point **Y** to point **Z**. For ease of reference, the corresponding endpoints **Y** and **Z** are labeled on the defect shown in **Figure 3**.

As seen in **Figure 4,** the length of the surface feature of the carrot defect is related to the thickness of the epitaxial layer and the off-axis angle α illustrated in **Figure 11**. In fact, the length of a carrot defect in the growth plane is inversely proportional to the tangent of the off-axis angle α.

In typical epitaxial growth systems that do not utilize the present invention, it is common to have a density of carrot defects in excess of 2.5 per square centimeter. The inventors have discovered that the density of carrot defects in an epitaxial layer of silicon carbide may be reduced by arresting the propagation of such defects during epitaxial growth. According to some embodiments of the present invention, propagation of carrot defects may be arrested by halting and/or reducing the flow of silicon and carbon source gases during normal epitaxial growth, etching a predetermined thickness of the grown epitaxial layer and resuming the flow of silicon and carbon source gases to resume growth of the epitaxial layer to the desired ultimate thickness. The process of etching and growing silicon carbide may be performed once or may be repeated multiple times.

When the flow of reaction gases is halted, the carrier or other gases still flowing tend to etch the epilayers that have been grown on the substrate **20**. Additionally, etchant gases may be introduced into the reaction chamber during the growth interruption. Accordingly, the process according to embodiments of the present invention may be carried out in-situ within the epitaxial deposition chamber. This result may have multiple benefits: the process may be carried out without removing the substrate from the growth chamber, which may be time consuming and potentially exposes the substrate to contamination; the process may be carried out without requiring additional equipment or facilities; and the process can be carried out without significantly reducing material throughput. Furthermore, in particular embodiments of the present invention, the first and second growth processes are carried out without an intervening growth process.

Despite the advantages of performing the etch in-situ, it may be necessary or desirable to remove the substrate from the epitaxial growth chamber and perform the etch in a separate system, particularly if the epitaxial deposition is done in a system other than a CVD system as described above. Thus, the scope of the invention includes both in-situ and ex-situ etching of the epitaxial layer.

In some embodiments, propagation of carrot defects is arrested within a highly doped buffer layer of the epitaxial structure, so that the carrot defects do not extend into more lightly doped layers that may, for example, form the active region of resulting devices. In this manner, the effect of carrot defects on device performance can be reduced or minimized. Moreover, by performing the etch/growth steps within a highly doped buffer layer, any deleterious effects of halting and restarting epitaxial growth may be reduced, minimized or even eliminated. The ensuing epitaxial layers that are primarily responsible for device performance may have a lower defect density as a result of carrot defect termination.

In specific embodiments, silicon carbide epitaxial growth is initiated to grow a highly doped buffer layer of silicon carbide. For example, growth of a silicon carbide epitaxial layer doped with nitrogen, phosphorus, boron and/or aluminum at a concentration of about 1E18 cm^{-3} or greater is initiated by flowing appropriate source gases (e.g. silane, propane and a dopant gas) through a CVD reactor along with a carrier gas. A first layer of silicon carbide is grown to a desired thickness. In some embodiments, the first layer is grown to a thickness of at least about 2.5 microns, however, the first layer may be grown thicker or thinner than 2.5 microns. In a typical embodiment, the first layer is grown to a thickness of about 4 microns. The source gases are then turned off or substantially reduced while the carrier gas continues to flow. While the source gases are shut off, the etchant and/or carrier gas etches the first epitaxial layer to reduce the thickness of the first epitaxial layer. The etchant gas may include H_2, HCl, Ar, Cl_2 and/or a carbon-containing gas such as propane. In the typical embodiment discussed above, the first epitaxial layer may, for example, be etched as much as about 3 microns. The inventors have found that carrot defects may be arrested when the first epitaxial layer is etched by as little as 0.4 microns.

The flow of source gases is then resumed, and a second epitaxial layer is grown on the first epitaxial layer (or the growth of the first epitaxial layer is resumed). The steps of halting the source gases, etching the grown epitaxial layer and restarting the source gases may be repeated multiple times. After the final etch step, the epitaxial layer may be capped with an additional epitaxial layer that, in some embodiments, includes about 2 microns of silicon carbide. The remainder of the epitaxial layers of the structure may then be grown. It has been found that by stopping the flow of source gases, etching the grown silicon carbide layer and growing additional silicon carbide on the etched surface, the majority of carrot defects propagating through the layer are terminated and do not continue to propagate in the subsequently grown layers.

Referring again to **Figure 4**, carrot defect termination is illustrated schematically therein in the case of carrot defect **B1**. As with carrot defect A1, carrot defect **B1** originates at the interface **12** between substrate **10** and epitaxial layer **20**. At a predetermined time after the initiation of growth, the flow of source gases is interrupted and growth of epitaxial layer **20** is halted. The epitaxial layer **20** then starts to be etched. After the epitaxial layer **20** is etched slightly, the flow of source gases is resumed at time t_1, and growth of epitaxial layer **20** continues until time t_2. As illustrated in **Figure 4**, the interruption of growth and etching of the epitaxial layer **20** causes carrot defect **B1** to terminate at interface **22.**

Although carrot defect **B1** is still present in epitaxial layer **20**, it may no longer affect the electrical characteristics of devices formed in subsequent epitaxial layers because it is terminated within the epitaxial layer **20**. Even though a terminated defect such as carrot defect **B1** may still give rise to a morphological feature on the surface of the epitaxial layer, the electrical impact of the defect may be minimized or eliminated.

However, in certain embodiments of the present invention, not all carrot defects are eliminated by the method of the invention. For example, as illustrated in **Figure 4**, some defects such as carrot defect A1 may continue to propagate through the growth interruption/etch/growth cycle at time t_1. Moreover, it is possible for new carrot defects to form after the growth interruption. However, significant reduction in the number of carrot defects that propagate to the surface of the epitaxial layer can be obtained.

Figure 5 is a Nomarski micrograph illustrating carrot defect termination according to aspects of the invention. The figure shows the surface of a 40 micron thick epitaxial layer. Two carrot defects are shown in close proximity in **Figure 5**. The lower carrot (**B2**) terminated at a growth interruption after 10 microns of growth. The upper carrot (**A2**) propagated through the entire 40 micron layer. Again, even though a morphological feature is visible in connection with carrot defect **B2**, the electrically active portion of the defect does not extend to the surface of the layer. The endpoints **Y, Z** of defect **A2** and endpoints **Y*, Z*** of defect **B2** are labeled for ease of comparison with defects **A1** and **B1** in the schematic diagram of **Figure 4**.

Other defect behavior has been observed. As discussed above, new carrot defects may originate at the growth interruption/etch step, as illustrated by defect **D1** in **Figure 6**. In addition, as indicated by defect **C1** in **Figure 6**, the threading dislocation **41** in the $\langle 0001 \rangle$ may be converted during the interruption/etch step into a basal plane dislocation **43** which propagates in approximately the $\langle 11\bar{2}0 \rangle$ direction resulting in the shape illustrated.

The defect behavior described above in connection with carrot defects **A1, B1**, **C1** and **D1** is illustrated in the micrographs of **Figures 7(A), 7(B), 7(C)** and **7(D).** In the process illustrated in **Figures 7(A)-(D)**, a layer of silicon carbide was epitaxially grown on a bulk substrate off-cut at an angle of about eight degrees towards the $\langle 11\bar{2}0 \rangle$ direction. After 10 microns of growth, the flow of source gases was interrupted, and the layers were etched by about one-half micron. Growth of the epitaxial layer was resumed, and the layer was grown an additional 30 microns. The layer was then etched with molten KOH to highlight defects in the material. **Figures 7(A)-(D)** are micrograph images of the etched layers.

Figure 7(A) illustrates a carrot defect similar to defect **A1** that continued to propagate through the growth interruption/etch step. The carrot defect extended a distance of 243 microns at the surface of the layer.

Figure 7(B) illustrates a carrot defect similar to defect **B1** that was terminated at the growth interruption/etch step. The carrot defect grew to a width of 62 microns before termination. It is noteworthy that the KOH etch did not etch a deep trench where the morphological remnant of the carrot appears, which indicates that the prismatic stacking fault did not propagate to the surface of the epitaxial layer.

Figure 7(C) illustrates a carrot defect similar to defect **C1** that was modified at the growth interruption/etch step such that the threading dislocation in the $\langle 0001 \rangle$ direction was converted to a dislocation propagating in approximately the $\langle 11\bar{2}0 \rangle$ direction.

Figure 7(D) illustrates a carrot defect similar to defect **D1** that originated at the growth interruption/etch step.

To examine the efficacy of the process, nearly identical wafers derived from the same SiC boule ("sister wafers") were processed with and without employing a process according to the invention. The carrot defect densities on each of the wafers were measured and compared. Since the number of carrot defects in a wafer is strongly dependent on the boule, it may be useful to compare carrot defect reduction in wafers taken from the same boule. For this comparison, the inventors calculated the ratio of the number of carrot defects in epilayers grown using the present invention to the number of carrot defects in epilayers grown without the invention, both on sister wafers. In each case, one set of wafers was grown without growth interruption/etching/growth cycle, while one set of wafers included an interruption/etching/growth cycle.

For each growth run, three wafers were loaded into a CVD reactor. The reactor was heated to growth temperature under a flow of carrier gas (H_2) only. At a temperature consistent with an etch-rate of approximately 3 microns/hour, growth of silicon carbide was initiated by introduction of silane (SiH_4) and propane (C_3H_8) reactant gases. Appropriate growth temperatures are system dependent and may be determined by a skilled person without undue experimentation.

In the control experiment, this growth was continued until a silicon carbide epitaxial layer of approximately 40 microns had been grown. In other experiments, growth was initiated in the same manner as the control experiment but was interrupted once or twice by stopping the flow of both the silane and propane. During that interruption of about 12 minutes duration, hydrogen in the carrier gas etched about 0.6 microns from the previously grown epitaxial layer. At the end of the growth interruption, silane and propane were reintroduced to resume growing silicon carbide.

In the first experiment, the initial epitaxial layer was approximately 5 microns thick, there was a single growth interruption, and the final epitaxial layer was approximately 35 microns thick. In the second experiment, the initial epitaxial layer was approximately 2.5 microns thick, there was a single growth interruption, and the final epitaxial layer was approximately 37.5 microns thick. In the third experiment, the initial epitaxial layer was approximately 2.5 microns thick, there were two growth interruptions with an additional 2.5 microns thick epitaxial layer between them, and the final epitaxial layer was approximately 35 microns thick. After growth, all of the carrots on each wafer were counted using a Nomarski microscope. The number of carrots on each wafer in the experimental runs was counted and compared to the number of carrots on its sister wafer in the control experiment. For purposes of the experiment, carrot defects were counted if they were not terminated within the epitaxial layer (i.e. if they continued to propagate to the surface). In each case, there was significant reduction in the number of carrot defects.

A histogram of the carrot reduction ratio is presented in **Figure 8**. The abscissa (x-axis) of **Figure 8** represents the ratio of carrot defect densities in wafers prepared using a process according to embodiments of the present invention to wafers that did not use such a process. The ordinate (y-axis) represents the percentage of samples falling within the indicated range of defect reduction Thus, **Figure 8** shows that the majority of wafers grown using the inventive process had only 10 to 30% of the number of carrot defects found in the control wafers. The median carrot density was reduced from 2.76 cm^{-2} to 0.67 cm^{-2}.

As illustrated in **Figure 8**, by using the process described above, the number of carrots can be reduced by roughly 70-80% of the expected value.

While the systems and methods have been described in relation to processes for depositing layers on substrates such as semiconductor wafers, the present invention may be employed in processes for depositing layers or the like on other types of substrates. The systems and methods of the present invention may be particularly useful in processes for forming an epitaxial layer on a substrate.

Various other modifications may be made in accordance with the invention. For example, heating systems may be used other than or in addition to inductive heating.

As used herein a "system" may include one or multiple elements or features. In the claims that follow, the "deposition system", the "deposition control system", the "buffer gas supply system", the "process gas supply system" and the like are not limited to systems including all of the components, aspects, elements or features discussed above or corresponding components, aspects, elements or features.

The foregoing is illustrative of the present invention and is not to be construed as limiting thereof. Although a few exemplary embodiments of this invention have been described, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the invention.

THAT WHICH IS CLAIMED IS:

1. A method of manufacturing a single crystal silicon carbide epitaxial layer on an off-axis silicon carbide substrate comprising:

growing a first layer of epitaxial silicon carbide on the substrate;

etching the first layer of epitaxial silicon carbide to reduce the thickness of the first layer; and

growing a second layer of epitaxial silicon carbide on the etched first layer of epitaxial silicon carbide.

2. A method according to Claim 1, further comprising interrupting the growth of the first layer of epitaxial silicon carbide prior to etching the first layer of epitaxial silicon carbide.

3. A method according to claim 2, wherein growing a first layer of epitaxial silicon carbide comprises flowing silicon and carbon containing source gases over the substrate and interrupting the growth of the first layer of epitaxial silicon carbide comprises reducing the flow of the source gases.

4. A method according to claim 2, wherein growing a first layer of epitaxial silicon carbide comprises flowing silicon and carbon containing source gases over the substrate and interrupting the growth of the first layer of epitaxial silicon carbide comprises halting the flow of the source gases.

5. A method according to claim 3, wherein etching the first layer of epitaxial silicon carbide comprises flowing an etchant gas over the substrate.

6. A method according to claim 5, wherein the etchant gas comprises H_2, Ar, HCl, Cl_2 and/or propane.

7. A method according to claim 1, wherein the first layer of epitaxial silicon carbide is doped with a dopant at a concentration of 1E18 cm^{-3} or greater.

8. A method according to claim 1, wherein the first layer of epitaxial silicon carbide has a thickness of less than 4 microns.

9. A method according to claim 1, wherein the first layer of epitaxial silicon carbide has a thickness of greater than 2 microns.

10. A method according to claim 1, wherein the first layer of epitaxial silicon carbide has a thickness of about 4 microns.

11. A method according to claim 1, wherein etching the first layer of epitaxial silicon carbide comprises etching the first layer of epitaxial silicon carbide by about 1 micron or more.

12. A method according to claim 1, wherein etching the first layer of epitaxial silicon carbide comprises etching the first layer of epitaxial silicon carbide by about 1 micron or less.

13. A method according to claim 1, wherein the second layer of epitaxial silicon carbide is grown to a thickness of about 2 microns.

14. A method according to claim 1, further comprising etching the second epitaxial layer, and growing a third epitaxial layer on the etched second epitaxial layer.

15. A method according to claim 14, further comprising interrupting the growth of the second epitaxial layer prior to etching the second epitaxial layer.

16. A method according to claim 1, wherein the substrate comprises silicon carbide having a polytype selected from the group consisting of 2H, 4H, and 6H.

17. A method according to claim 1, wherein etching the first layer of epitaxial silicon carbide comprises etching the first layer of epitaxial silicon carbide within the epitaxial growth reactor.

18. A method according to claim 1, wherein etching the first layer of epitaxial silicon carbide comprises removing the substrate from the epitaxial growth reactor and etching the first layer of epitaxial silicon carbide outside the epitaxial growth reactor.

19. A method according to claim 1, wherein the first epitaxial layer and the second epitaxial layer provide a buffer layer on the substrate.

20. A method according to claim 1, wherein growing a first layer of epitaxial silicon carbide on the substrate comprises growing a first layer of epitaxial silicon carbide on an epitaxial layer on the substrate.

21. A semiconductor structure comprising a silicon carbide epitaxial layer having a carrot defect which is terminated within the epitaxial layer.

22. A semiconductor structure comprising:

an off-axis silicon carbide substrate;

an epitaxial layer of silicon carbide on the substrate,

a carrot defect having a nucleation point in the vicinity of an interface between the substrate and the epitaxial layer, wherein the carrot defect terminates within the epitaxial layer.

23. A structure according to claim 22, wherein the substrate comprises silicon carbide having a polytype selected from the group consisting of 2H, 4H, and 6H.

24. A structure according to claim 22, wherein the silicon carbide substrate is cut off-axis towards the $\left\langle 11\bar{2}0 \right\rangle$ direction.

25. A structure according to claim 22, wherein the silicon carbide substrate is cut off-axis towards a crystallographic direction perpendicular to the c-axis.

26. A structure according to claim 22, wherein the epitaxial layer comprises a buffer layer.

27. A structure according to claim 22, wherein the epitaxial layer is doped with a dopant at a concentration of 1E18 cm^{-3} or greater.

28. A structure according to claim 27, wherein the dopant comprises nitrogen, phosphorus, boron or aluminum.

REDUCTION OF CARROT DEFECTS IN SILICON CARBIDE EPITAXY

ABSTRACT

Single crystal silicon carbide epitaxial layer on an off-axis substrate are manufactured by placing the substrate in an epitaxial growth reactor, growing a first layer of epitaxial silicon carbide on the substrate, interrupting the growth of the first layer of epitaxial silicon carbide, etching the first layer of epitaxial silicon carbide to reduce the thickness of the first layer, and regrowing a second layer of epitaxial silicon carbide on the first layer of epitaxial silicon carbide. Carrot defects may be terminated by the process of interrupting the epitaxial growth process, etching the grown layer and regrowing a second layer of epitaxial silicon carbide. The growth interruption/etching/regrowth may be repeated multiple times. A silicon carbide epitaxial layer has at least one carrot defect that is terminated within the epitaxial layer. A semiconductor structure includes an epitaxial layer of silicon carbide on an off-axis silicon carbide substrate, and a carrot defect having a nucleation point in the vicinity of an interface between the substrate and the epitaxial layer and is terminated within the epitaxial layer.

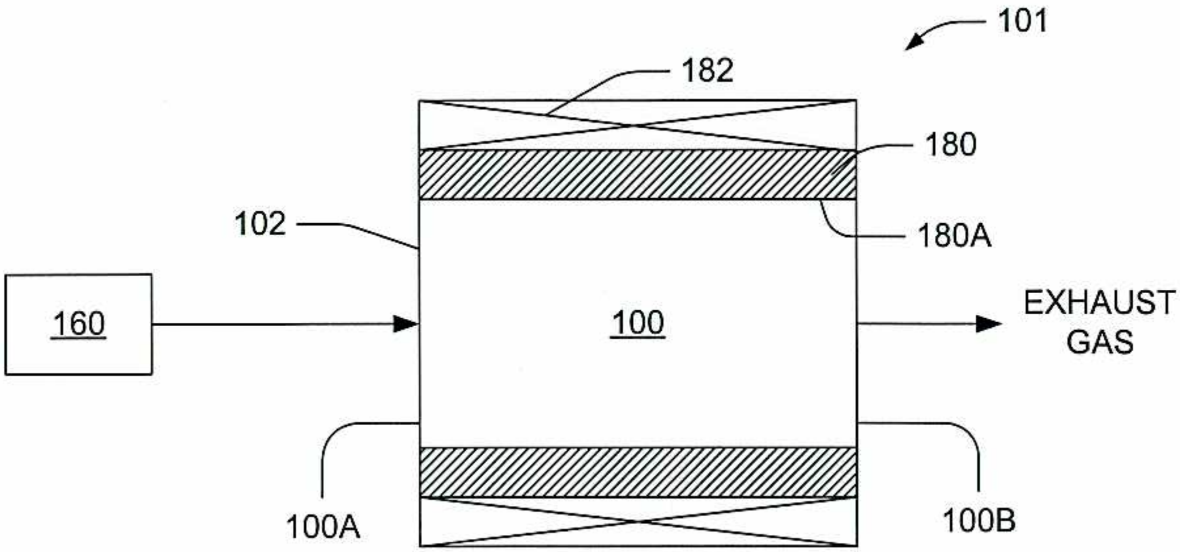

FIGURE 1

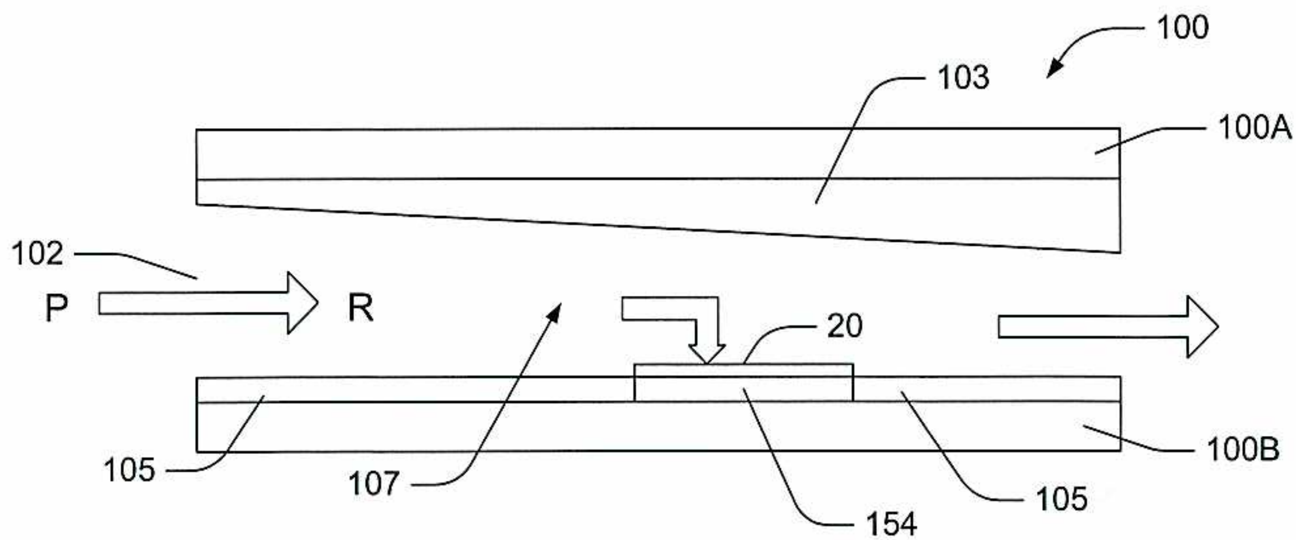

FIGURE 2

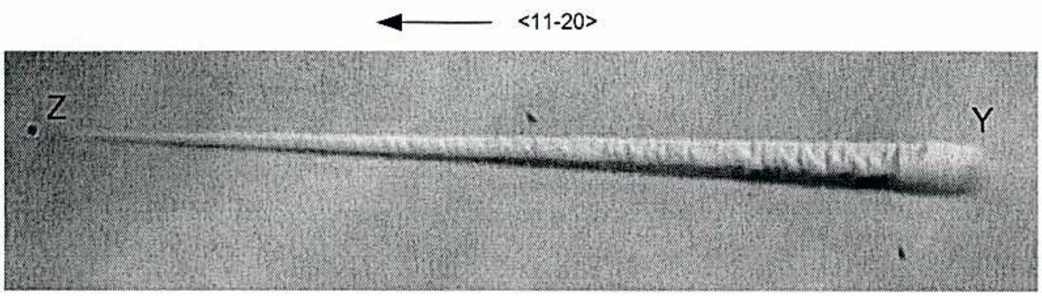

FIGURE 3

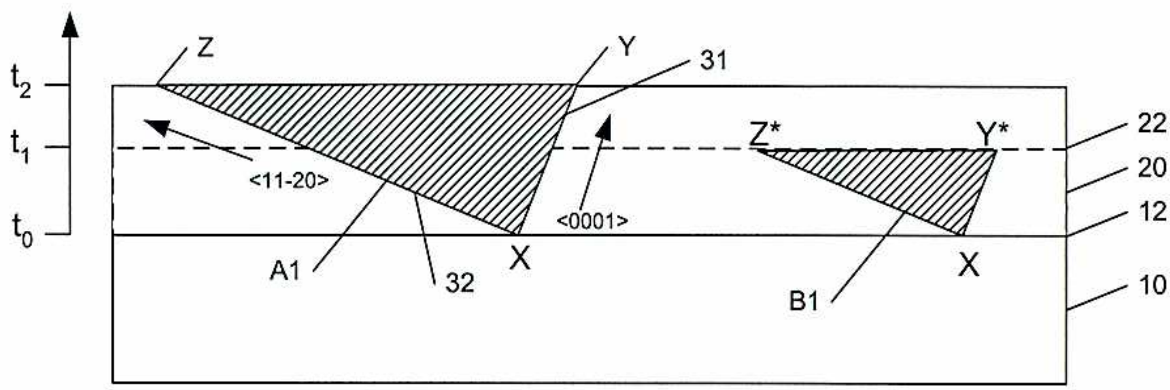

FIGURE 4

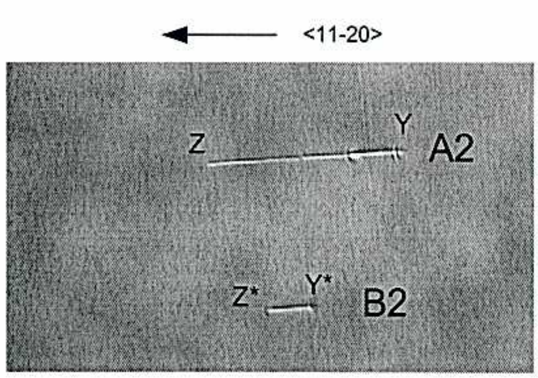

FIGURE 5

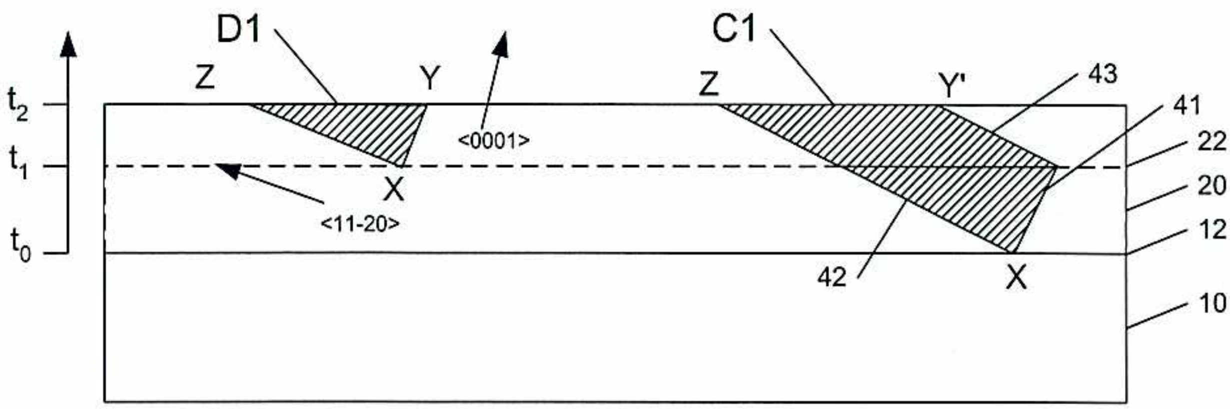

FIGURE 6

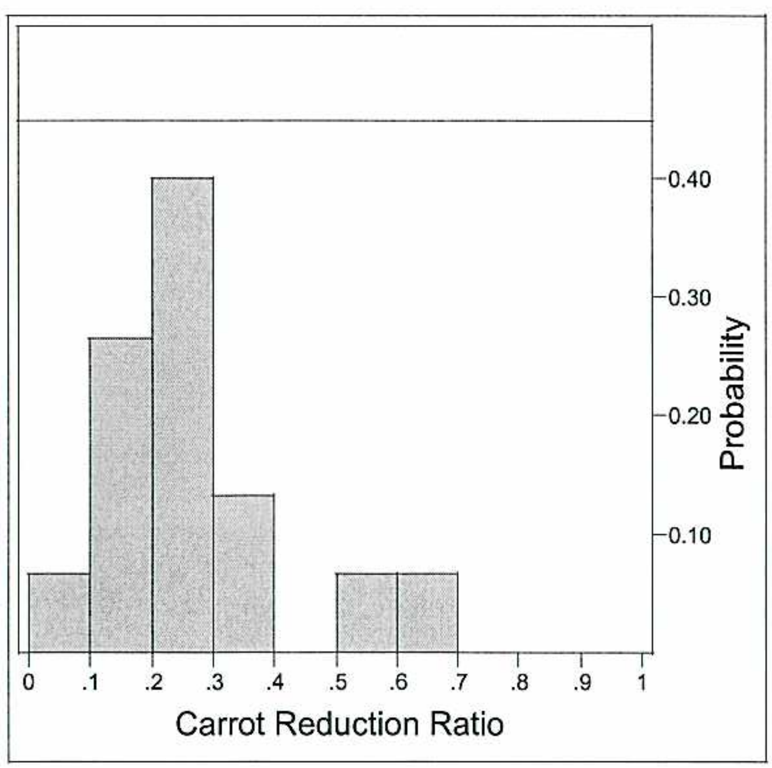

FIGURE 8

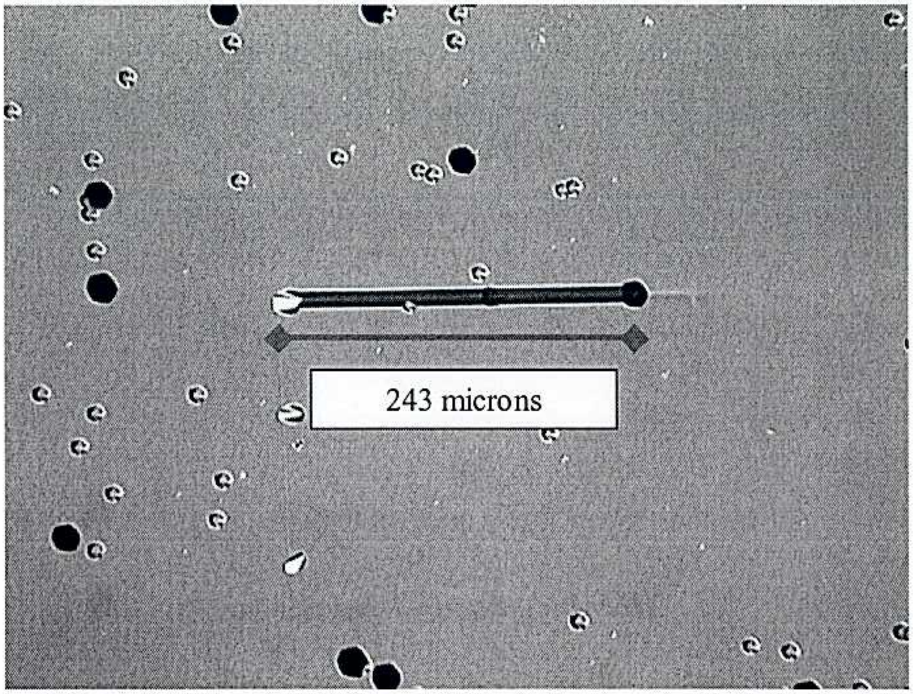

FIGURE 7(A)

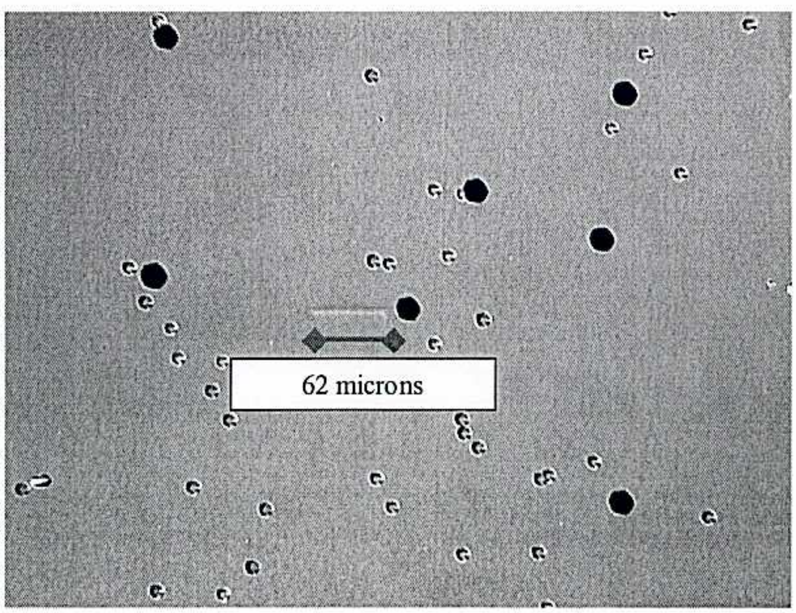

FIGURE 7(B)

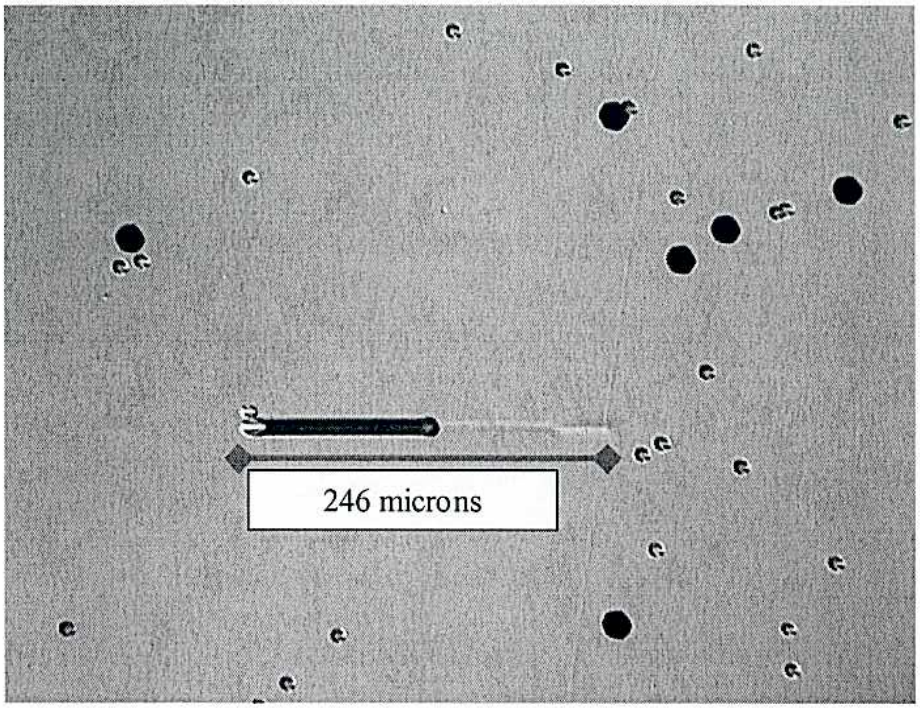

FIGURE 7(C)

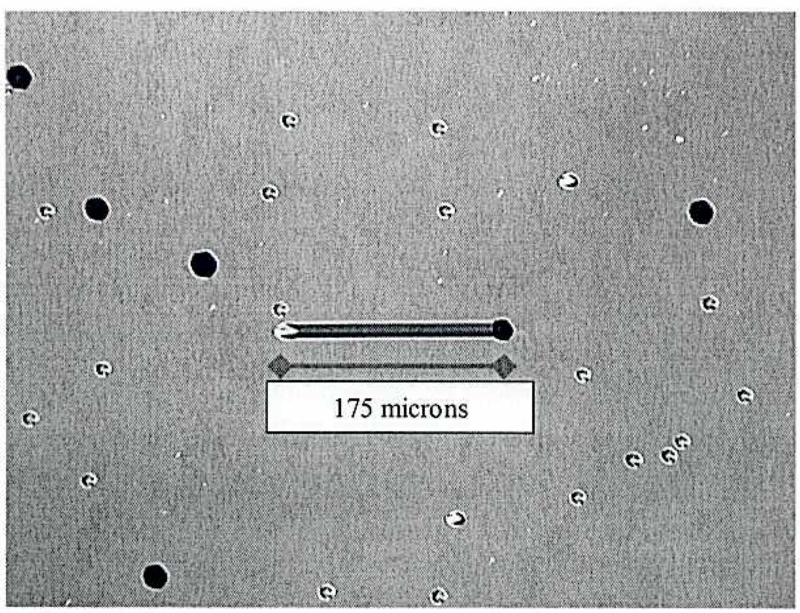

FIGURE 7(D)

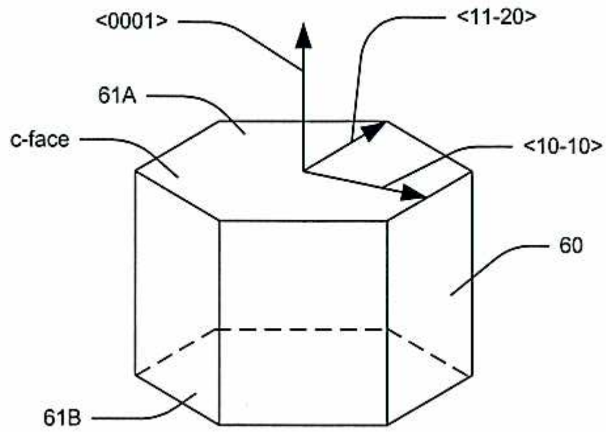

FIGURE 9

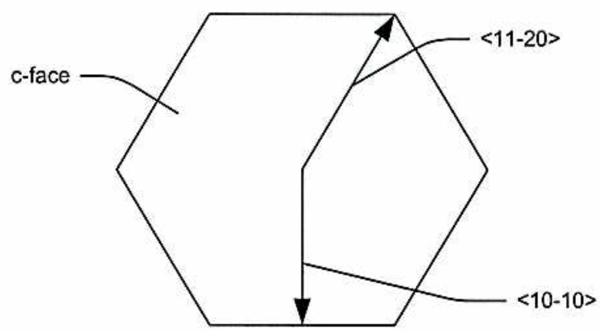

FIGURE 10

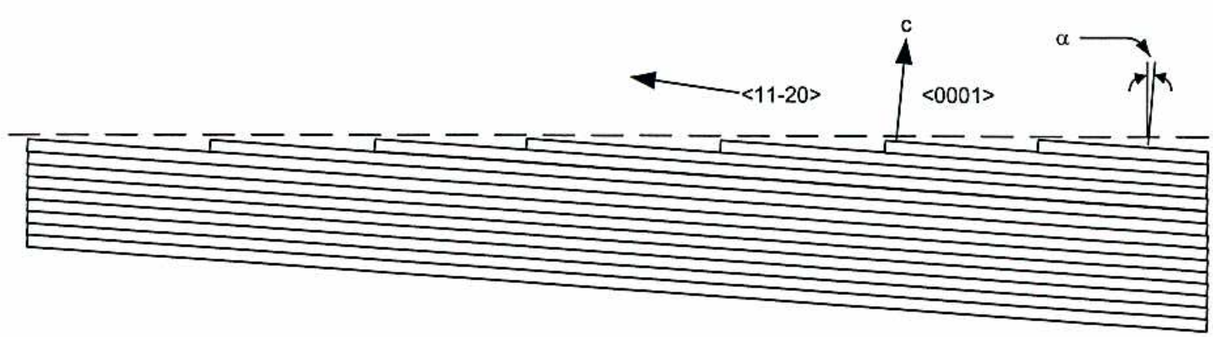

FIGURE 11

Attorney Docket No. 5000.419 **PATENT**

IN THE UNITED STATES PATENT OFFICE

In re: Valeri F. Tsvetkov et al.
App. No. 10/990,607
Filing Date: November 17, 2004
For: REDUCTION OF SUBSURFACE DAMAGE
IN THE PRODUCTION OF BULK SiC CRYSTALS

April 28, 2005

Mail Stop Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to action on the merits, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

In re: Davis A. McClure et al.
App. No. 11/022,496
Filing Date: December 22, 2004
Page 2

Amendment to the Specification:

Please add the following new paragraph to the beginning of the specification:

[001] This invention was developed under Office of Naval Research/DARPA Contract No. N00014-02-C-0302. The government may have certain rights in this invention.

Respectfully submitted,

[redacted]
Reg. No. 54,717

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S:\FIRM DOCS\5000\419\Preliminary Amendment 042705.DOC

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on April 28, 2005 and is addressed to Mail Stop Amendments, Commissioner for Patents, P.O.Box 1450, Alexandria, VA 22313-1450.

[redacted]
Deborah Dossinger

Reduction Of Subsurface Damage In The Production Of Bulk SiC Crystals

Background of the Invention

[0001] The present invention relates to the growth of silicon carbide for semiconductor purposes, and to the seeded sublimation growth of large, high quality silicon carbide single crystals. The invention particularly relates to improvements that reduce the defect density in large single crystals grown using seeded sublimation techniques.

[0002] Silicon carbide has found use as a semiconductor material for various electronic devices and purposes in recent years. Silicon carbide is especially useful due to its physical strength and high resistance to chemical attack. Silicon carbide also has excellent electronic properties, including radiation hardness, high breakdown filed, a relatively wide band gap, high saturated electron drift velocity, high temperature operation, and absorption and emission of high energy photons in the blue, violet, and ultraviolet regions of the spectrum.

[0003] Single crystal SiC is often produced by a seeded sublimation growth process. In a typical silicon carbide growth technique, a seed crystal and a source powder are both placed in a reaction crucible which is heated to the sublimation temperature of the source and in a manner that produces a thermal gradient between the source and the marginally cooler seed crystal. The thermal gradient encourages vapor phase movement of the materials from the source to the seed followed by condensation upon the seed and the resulting bulk crystal growth. The method is also referred to as physical vapor transport (PVT).

[0004] In a typical silicon carbide growth technique, the crucible is made of graphite and is heated by induction or resistance, with the relevant coils and insulation being placed to establish and control the desired thermal gradients. The source powder is silicon carbide, as is the seed. The crucible is oriented vertically, with the source powder in the lower portions and the seed positioned at the top, typically on a seed holder; see U.S. Patent No. 4,866,005 (reissued as No. RE34,861). These sources are exemplary, rather than limiting, descriptions of modern seeded sublimation growth techniques.

[0005] Current seeded sublimation techniques for the production of large bulk single crystals of SiC typically result in a high concentration of defects on the growing surface of the SiC crystal. High concentrations of defects cause significant problems in limiting the performance characteristics of devices made on the crystals, or substrates resulting from the crystals. For example, a typical micropipe defect density in some commercially available silicon carbide wafers can be on the order of 100 per square centimeter (cm^{-2}). A megawatt device formed in silicon carbide, however, requires a micropipe defect free area on the order of 0.4 cm^{-2}. Thus, obtaining large single crystals that can be used to fabricate large surface area devices for high-voltage, high current applications remains difficult.

[0006] Common defects found in crystals produced in the seeded sublimation production of SiC crystals include screw dislocations, particularly 1c screw dislocations. The nature and description of specific defects is generally well understood in the crystal growth art. In particular, a screw dislocation is defined as one in which the Burgers Vector is parallel to the direction vector. On an atomic scale, the resulting dislocation gives the general appearance of a spiral staircase. Other defects include threading dislocations, basal plane dislocations and micropipes. Clusters of 1c screw dislocations result in micropipes. These defects are present in crystal seeds as background defects, originating at the bottom of the seed and migrating to the surface.

[0007] More defects are introduced as a result of mechanical polishing of the surface of the crystal seed. These newly introduced defects typically reach 5-10 microns below the polished surface and are sometimes referred to as "subsurface defects." They have characteristics of 1c or threading edge or basal plane defects, but tend to loop back to the crystal surface. If these defects remain in the seed crystal, they will tend to propagate into the growing crystal under growth conditions.

[0008] The presence of subsurface defects in bulk single crystals of SiC may also interfere with single-polytype crystal growth. The 150 available polytypes of SiC raise a particular difficulty. Many of these polytypes are very similar, often separated only by small thermodynamic differences. Maintaining the desired polytype identity throughout the crystal is only one difficulty in growing SiC crystals of large sizes in a seeded sublimation system. When surface defects are present, there is not enough polytype information on the crystal surface for depositing layers to maintain the desired polytype. Polytype changes on the surface of the growing crystal result in the formation of even more surface defects.

[0009] One technique used to remove such defects is hydrogen etching of the seed wafer at temperatures of 1600 °C or greater. Hydrogen etching, however, is a difficult and expensive process, and often results in etching of the silicon face of the seed as well as the growing surface of the seed. An etched Si face is undesirable because the etching process may enlarge pits and micropipes on the Si face, or create new ones, or both. Under growth conditions, these defects may then transmit as open void spaces through the seed into the growing crystal.

[0010] Another problem with current etching technology is that the etching is only efficient to depths of about 1 μm. It is estimated that subsurface damage resulting from the crystal growth process reaches depths of at least about 5 μm, and possibly deeper than about 10 μm. If these defects are not removed, the resultant devices grown on the SiC seed will have an unacceptable defect level.

[0011] Accordingly, it would be desirable to develop a method for efficiently removing subsurface damage on the growing surface of bulk single crystals of SiC, while protecting the opposing crystal face in order to produce large, high quality bulk single crystals of SiC.

Summary of the Invention

[0012] The invention is an improvement in a method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system. In one aspect, the invention is a method of protecting a 0001 Si face of a SiC seed during a KOH etch of the 0001 C face of the SiC seed.

[0013] In another aspect, the invention is a method for efficiently removing subsurface damage on the growing surface of bulk single crystals of SiC, while protecting the opposing crystal face in order to produce large, high quality bulk single crystals of SiC.

[0014] The invention is also a SiC seed structure comprising a first 0001 Si face on a first SiC seed directly against a second 0001 Si face on a second SiC seed.

[0015] The foregoing, as well as other objectives and advantages of the invention and the manner in which the same are accomplished, is further specified within the following detailed description and its accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figure 1 is a cross sectional schematic diagram of a sublimation system for seeded sublimation growth;

[0017] Figure 2 is a schematic illustration of a SiC seed prepared in accordance with the present invention and attached to a seed holder; and

[0018] Figure 3 is a schematic illustration of a SiC seed structure prepared in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] The present invention relates to a method for producing high quality bulk single crystals of silicon carbide. In particular, the present invention incorporates several techniques for improving the growth of such crystals using seeded sublimation. The invention is described in terms of the sublimation growth of silicon carbide, but is not limited to silicon carbide per se.

[0020] As noted in the background portion of the specification, the general aspects of seeded sublimation growth of silicon carbide have been generally well established for a number of years. Furthermore, those familiar with the growth of crystals, particularly in difficult material systems such as silicon carbide, will recognize that the details of a given technique can and will vary, usually purposefully, depending upon the relevant circumstances. Accordingly, the descriptions given herein are most appropriately given in a general and schematic sense with the recognition that those persons of skill in this art will be able to carry out the improvements of the invention based on the disclosures herein without undue experimentation.

[0021] In a first broad aspect, the invention is an improvement in a method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system. The improvement includes etching the front face on each of a first and second SiC seed to a depth of greater than about 20 μm while protecting the opposite or back face on each of the first and second SiC faces. Protection of the back faces occurs by placing the faces sufficiently close to one another to shield the back faces from being etched during etching of the respective unprotected front faces. In preferred embodiments, the first and second back faces are placed directly against one another. Separation of the first and second SiC seeds occurs after the etching of the front faces is complete. As used herein, the front face is defined as the growing face of the crystal, and the back face is defined as the face of the crystal opposite the front face. The invention is described in terms of the 0001 Si face and the 0001 C face of the crystal for ease of discussion, but is not limited to these faces.

[0022] In another aspect, the invention is a method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system. The method includes protecting a first 0001 Si face on a first SiC seed and a second 0001 Si face on a second SiC seed by placing them sufficiently close to one another to shield the 0001 faces from being etched during etching of the respective unprotected 0001 C faces. Next, the 0001 C faces are prepared for growth by etching a 0001 C face on each of the first and second SiC seeds to a depth of greater than about 20 μm while protecting the first and second 0001 Si faces. The method further includes separation of the first and second seeds, followed by attachment of the unetched first 0001 Si face on the first SiC seed to a seed holder. Next, SiC growth on the etched 0001 C face of the SiC seed is initiated by placing the seed holder and SiC source powder in a crucible, evacuating the crucible to remove ambient air and other impurities; placing the crucible under inert gas pressure, heating the system to SiC growth temperatures, and reducing the pressure of the system.

[0023] In another aspect, the invention is a method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system by reducing the presence of subsurface damage, for example 1c screw dislocations at a crystal growth face. Without being bound by theory, it is believed that subsurface damage can be reduced by protecting a first 0001 Si face on a first SiC seed by placing the seeds sufficiently close to one another to shield the 0001 Si faces from being etched during etching of the respective unprotected 0001 C faces, etching a 0001 C face on each of the first and second SiC seeds to a depth sufficient to remove the 1c screw dislocations ,basal plane dislocations and threading dislocations induced by the polishing process while protecting the first and second 0001 Si faces; separating the first and second SiC seeds, and thereafter initiating sublimation growth of silicon carbide on the etched 0001 C face of the SiC seed crystal.

[0024] In yet another aspect, the invention is a method for reducing the presence of subsurface damage on the growth face of a high quality bulk single crystal silicon carbide during seeded sublimation growth. The method includes protecting a first 0001 Si face on a first SiC seed and a second 0001 Si face on a second SiC seed by placing them sufficiently close to one another to shield the 0001 Si faces from being etched during etching of the respective unprotected 0001 C faces, and thereafter etching a 0001 C face on each of the first and second SiC seeds to a depth sufficient to remove subsurface damage while protecting the first and second 0001 Si faces. After etching, separation of the seeds and attachment of the unetched first 0001 Si face on the first SiC seed to a seed holder prepares the seed for sublimation growth. The second 0001 Si face on the second SiC seed may be attached to a second seed holder, thereby preparing the second SiC seed for sublimation growth.

[0025] In yet another method, the invention is a method of protecting a 0001 Si face of a SiC seed during etching. The method includes placing a first 0001 Si face on a first SiC seed sufficiently close to a second 0001 Si face on a second SiC seed to prevent etching of the first and second 0001 Si faces during a KOH etch of a first 0001 C face on the first SiC seed and a second 0001 face on the second SiC seed, and thereafter separating the unetched first and second 0001 Si faces.

[0026] The etching step is preferably a molten KOH etch. KOH etches are known in the art, however the 0001 Si face of the SiC seed is pitted by the enhanced etching rate associated with micropipes and other defects. In the present invention, protection of the 0001 Si faces of the SiC seeds during the KOH etch process results in a sufficiently etched 0001 C face on each seed and a 0001 Si face maintains its unetched condition. In a preferred embodiment, the KOH etch is conducted in a melt at a temperature of about 600 ˚C and is at least about 20 μm deep, more preferably greater than about 25 μm deep, and most preferably greater than about 30 μm deep. A preferred etch depth is between about 20 and 45 μm. There is no limitation to how deep the KOH etch may be, but relevant subsurface damage, such as that described in the Background section, is effectively removed at these depths, and etching beyond about 45 μm, although not harmful, is unnecessary.

[0027] Although a KOH etch is preferred, in alternative embodiment, the protected seeds may be etched in a hydrogen etch at temperatures around about 1600 ˚C or by a chemo-mechanical polish of the seed of the type that does not produce the damage described earlier.

[0028] Figure 1 is a cross sectional schematic diagram of a sublimation system for seeded sublimation growth of the type contemplated as useful in the present invention. The system is broadly designated at 10. As in most typical systems, the system 10 includes a graphite susceptor, or crucible, 12 and a plurality of induction coils 14 that heat the susceptor 12 when current is applied through the coils 14. Alternatively, some systems incorporate resistance heating. It will be understood by those familiar with these crystal growth techniques that the system can be further enclosed in some circumstances, *e.g.*, in a water-cooled quartz vessel. Such further enclosures are, however, less relevant to the invention and are omitted herein to help clarify the drawing and description. Additionally, those persons skilled in this art recognize that silicon carbide sublimation systems of the type described herein are available both commercially and as constructed in a custom fashion as may be necessary or appropriate. They accordingly can be selected or designed by those of ordinary skill in this art without undue experimentation.

[0029] The susceptor 12 is typically surrounded by insulation 16, several portions of which are illustrated in Figure 1. Although Figure 1 illustrates the insulation as being generally consistent in size and placement, it will be understood and is recognized by those of skill in the art that the placement and amount of the insulation 16 can be used to provide desired thermal gradients (both axially and radially) along the susceptor 12. Again, for purposes of simplification, these possible permutations are not illustrated herein.

[0030] The susceptor 12 includes one or more portions for containing a silicon carbide powder source 18. Such a powder source 18 is most commonly—although not exclusively—used in seeded sublimation growth techniques for silicon carbide. Figure 1 illustrates the powder source 18 as being contained in a lower portion of the susceptor 12 and this is one typical arrangement. As another familiar variation, some systems distribute the source powder in a vertical, cylindrical arrangement in which the source powder surrounds a larger portion of the interior of the susceptor 12 than does the arrangement illustrated in Figure 1. The invention described herein can be appropriately carried out using both types of equipment.

[0031] The silicon carbide seed crystal is designated at 20, and is typically placed in upper portions of the susceptor 12. A seed holder 22 typically holds the seed 20 in place with the seed holder 22 being attached to the susceptor in an appropriate fashion. The seed 20 is typically attached to the seed holder 22 via the unetched 0001 Si face. In the orientation illustrated in Figure 1, the upper portions of the seed holder 22 would typically be attached via attachment means known in the art to the uppermost portions of the susceptor 12 to hold the seed 20 in the desired position. The seed holder 22 is preferably a graphite seed holder.

[0032] In some embodiments it may be desirable to anneal the seed holder 22 prior to attaching the seed 20. Annealing the seed holder 22 prior to sublimation growth prevents the seed holder 22 from undergoing significant distortion during crystal growth at SiC sublimation temperatures. Annealing the seed holder 22 also minimizes or eliminates temperature differences across the seed 20 that would otherwise tend to initiate and propagate defects in the growing crystal 24. A preferred process for annealing the seed holder 22 includes annealing at temperatures at or about 2500 °C for at least about 30 minutes.

[0033] The growing crystal is illustrated by the dotted rectangle designated 24. The growing crystal 24 may have the same diameter as the seed 20 or a larger diameter than the seed 20. Preferably, the growing single crystal 24 has the same diameter as the seed 20.

[0034] The general scheme for sublimation growth is set forth briefly in the Background portion of the specification, as well as in other sources well-known to those of ordinary skill in this art. Typically, an electric current, having a frequency to which the susceptor 12 responds, is passed through the induction coils 14 to heat the graphite susceptor 12. The amount and placement of the insulation 16 are selected to create a thermal gradient between the powder source 18 and the growing crystal 24 when the susceptor 12 heats the powder source 18 to sublimation temperatures, which are typically on the order of between about 2000 °C and 2500 °C. The thermal gradient is established to maintain the temperature of the seed 20 and thereafter the growing crystal 24 below temperature of silicon carbide powder to thereby thermodynamically encourage the vaporized species that are generated when silicon carbide sublimes (Si, Si_2C, and SiC_2) to condense first upon the seed crystal and thereafter upon the growing crystal. As one example, U.S. Patent No. 4,866,005 suggests maintaining the seed at about 2300 °C. Sublimation growth may also be conducted at temperatures between about 2000 and 2500 °C and may be on-axis or off-axis growth. Preferably, the sublimation growth is on-axis growth.

[0035] Preferably, the susceptor 12 is placed under gas pressure prior to initiating sublimation growth. Preferred gases include noble gases, nitrogen, CO, H_2, CH_4, other hydrocarbons known in the art, and mixtures thereof.

[0036] After reaching the desired crystal size, growth is terminated by reducing the temperature of the system to below about 1900 °C and raising the pressure to above about 400 torr.

[0037] It may be further desirable to anneal the crystal after completion of the sublimation growth process. The crystal may be annealed at temperatures above about 2500 °C for a period greater than about 30 minutes.

[0038] In some embodiments, it may be preferred to include dopant atoms in the single crystal 24. Introducing dopant gases to the seeded sublimation system incorporates dopant atoms in the single crystal 24. Dopants are selected for their acceptor or donor capabilities. Donor dopants are those which produce n-type conductivity in the crystal and acceptor dopants are those which produce p-type conductivity in the crystal. Preferred dopant atoms include donor and acceptor dopant atoms. Especially preferred donor dopants include N, P, As, Sb, Bi, and mixtures thereof. Especially preferred acceptor dopants include B, Al, Ga, In, Tl, and mixtures thereof.

[0039] For purposes of clarity, the singular term, "thermal gradient," will be used herein, but it will be understood by those of skill in this art that several gradients can desirably co-exist in the susceptor 12 and can be subcategorized as axial and radial gradients, or as a plurality of isotherms.

[0040] If the temperature gradients and other conditions (pressure, carrier gases, etc.) are properly maintained, the overall thermodynamics will encourage the vaporized species to condense first on the seed crystal 20 and then on the growing crystal 24 in the same polytype as the seed crystal 20.

[0041] In describing the invention, it will be understood that a number of techniques are disclosed. Each of these has individual benefit, and each can also be used in conjunction with one or more, or in some cases all, of the other disclosed techniques. Accordingly, for the sake of clarity, this description will refrain from repeating every possible combination of the individual steps in an unnecessary fashion. Nevertheless, the specification and claims should be read with the understanding that such combinations are entirely within the scope of the invention and the claims.

[0042] In considering the proportional dimensions of the diameter and thickness of the seed crystal, whether expressed as a percentage, a fraction, or a ratio, it will be understood that in the context of the improvements provided by the invention, these proportions have their inventive meaning in the context of the larger-diameter seed crystals that are described herein.

[0043] Accordingly, in certain embodiments the invention is described and claimed herein in the relevant embodiments in a manner that includes the absolute dimensions of the crystal, usually in terms of a diameter, of which 2 inch, 3 inch, and 100 mm diameter single crystals are preferred.

[0044] In one aspect, and as seen in Figure 2, the invention is a SiC seed 20 with low density of 1c screw dislocations and threading dislocations on a growing surface 26. The seed has an unetched 0001 Si face 28 and an etched 0001 C face 26 having a 1c screw dislocation density of less than about 2000 cm^{-2}.

[0045] The SiC seed may be attached to a seed holder 22, preferably a graphite seed holder. The attachment may be any attachment known in the art. In one embodiment, a mechanical attachment may be preferred. Preferably, the attachment of the SiC seed to the seed holder occurs via the unetched 0001 Si face of the seed.

[0046] In yet another aspect, and as depicted in Figure 3, the invention is a SiC seed structure, broadly designated at 30 having a first 0001 Si face 32 on a first SiC seed 34 directly against a second 0001 Si face 36 on a second SiC seed 38. The first 0001 Si face 32 is directly opposite a first 0001 C face 40 and the second 0001 Si face 36 is directly opposite a second 0001 C face 42. Preferably, any gaps between the first 0001 Si face 32 on the first SiC seed 34 and the second 0001 Si face 36 on the second SiC seed 38 are less than about 10 μm, more preferably less than about 5 μm, and most preferably less than about 2 μm.

[0047] Bulk single crystals grown in accordance with the present invention have reduced surface and subsurface damage. Preferably, the growth surface is substantially free of subsurface damage.. The growth surface of crystals grown in accordance with the present invention allows the crystal to maintain a consistent polytype throughout the crystal. Preferred polytypes include the 3C, 4H, 6H, and 15R polytypes.

EXAMPLE

[0048] In one example, two 3.25 inch polished SiC seed wafers were placed together, 0001 Si face to 0001 Si face to prevent the silicon faces from etching in a KOH melt and so keep them flat to ensure perfect thermal contact of the seed with the seed holder during crystal growth. The two seeds were placed in a KOH melt at 600 °C for 45 minutes to allow etching of the 0001 C faces on the SiC wafers. This etching removed 35 μm from the 0001 C faces. After the etch, the seeds were wafered and polished as known in the art, and the 1c screw dislocation density in the wafer near the seed was 2000 cm^{-2}, which is five times lower than the typical 1c screw dislocation density in the crystal grown on the polished seed.

[0049] In the specification and the drawings, typical embodiments of the invention have been disclosed. Specific terms have been used only in a generic and descriptive sense, and not for purposes of limitation. The scope of the invention is set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. In a method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system, the improvement comprising:

etching a front face on each of a first and second SiC seed to a depth of greater than about 20 μm while protecting a back face on each of the first and second SiC seeds by placing the first and second back faces sufficiently close to one another to shield the back faces from being etched during etching of the respective unprotected front faces; and

thereafter separating the first and second SiC seeds.

2. A method according to claim 1 further comprising the step of attaching an unetched back face to a seed holder.

3. A method according to claim 1 wherein the step of protecting a first back face on a first SiC seed and a second back face on a second SiC seed by placing them close enough to one another to prevent etching of the first and second back faces comprises placing the first back face directly against the second back face.

4. A method according to claim 1 comprising etching the front face on each of the first and second SiC seeds with KOH.

5. A method according to claim 2 wherein the step of attaching the unetched back face to a seed holder is followed by placing the seed holder in a crucible and initiating sublimation growth on the etched front face.

6. A method according to claim 5 wherein the step of initiating sublimation growth on the etched front face comprises initiating on-axis sublimation growth.

7. A method according to claim 6 wherein the step of initiating sublimation growth comprises growing a bulk single crystal at substantially the same diameter as the seed crystal.

8. A method according to claim 1 wherein the front face is 0001C and the back face is 0001Si.

9. A method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system, the method comprising:

protecting a first 0001 Si face on a first SiC seed and a second 0001 Si face on a second SiC seed by placing them sufficiently close to one another to shield the 0001 faces from being etched during etching of the respective unprotected 0001 C faces;

etching a 0001 C face on each of the first and second SiC seeds to a depth of greater than about 20 μm while protecting the first and second 0001 Si faces;

separating the first and second SiC seeds;

thereafter attaching the unetched first 0001 Si face on the first SiC seed to a seed holder

placing the seed holder in a crucible;

placing SiC source powder in the crucible

evacuating the crucible to remove ambient air and other impurities;

placing the crucible under gas pressure;

heating the system to SiC growth temperatures; and

reducing the pressure to initiate SiC growth.

10. A method according to claim 9 comprising etching the 0001 C face on each of the first and second SiC seeds with KOH.

11. A method according to claim 9 wherein the step of attaching the unetched first 0001 Si face to a seed holder comprises placing the seed on a graphite seed holder.

12. A method according to claim 9 further comprising stopping growth by raising the inert gas pressure in the crucible to above about 400 torr and lowering the temperature to below about 1900 °C to stop crystal growth.

13. A method according to claim 9 wherein the step of placing the crucible under gas pressure involves introducing a gas selected from the group consisting of noble gases, CO, H_2, CH_4, N_2, and mixtures thereof.

14. A method according to claim 9 wherein the step of heating the system to SiC growth temperatures involves heating to temperatures between about 1900 and 2500 °C.

15. A method according to claim 9 further comprising the step of introducing dopant gases to the seeded sublimation system, thereby incorporating dopants into the SiC single crystal.

16. A method according to claim 9 further comprising annealing the crystal after the completion of the crystal growth process.

17. A method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system, the method comprising:

reducing the presence of 1c screw dislocations at a crystal growth surface by protecting a first 0001 Si face on a first SiC seed and a second 0001 Si face on a second SiC seed by placing the seeds sufficiently close to one another to shield the 0001 Si faces from being etched during etching of the respective unprotected 0001 C faces;

etching a 0001 C face on each of the first and second SiC seeds to a depth sufficient to remove subsurface damage while protecting the first and second 0001 Si faces;

separating the first and second SiC seeds; and

initiating sublimation growth of silicon carbide on the etched 0001 C face of the SiC seed crystal.

18. A method according to claim 17 wherein said step of etching a 0001 C face to a depth sufficient to remove subsurface damage comprises etching to a depth greater than about 20 μm.

19. A method according to claim 17 further comprising the step of attaching the unetched second 0001 Si face to a second seed holder.

20. A method according to claim 17 wherein the step of protecting a first 0001 Si face on a first SiC seed and a second 0001 Si face on a second SiC seed by placing them close enough to one another to prevent etching comprises placing the first 0001 Si face directly adjacent the second 0001 Si face.

21. A method according to claim 17 comprises etching a 0001 C face on each of the first and second SiC seeds with KOH.

22. A method according to claim 17 wherein the step of initiating sublimation growth on the etched 0001 C face comprises initiating on-axis sublimation growth.

23. A method according to claim 22 wherein the step of initiating sublimation growth comprises growing a bulk single crystal at substantially the same diameter as the seed crystal.

24. A method according to claim 17 further comprising annealing the seed holder prior to sublimation growth to prevent the seed holder from significant distortion during crystal growth at SiC sublimation temperatures and thereby minimize or eliminate

temperature differences across the seed that would otherwise tend to initiate and propagate defects in the growing crystal.

25. A method for reducing the presence of subsurface damage on the growth face of a high quality bulk single crystal silicon carbide during seeded sublimation growth, the method comprising:

protecting a first 0001 Si face on a first SiC seed and a second 0001 Si face on a second SiC seed by placing them sufficiently close to one another to shield the 0001 Si faces from being etched during etching of the respective unprotected 0001 C faces;

etching a 0001 C face on each of the first and second SiC seeds to a depth sufficient to remove subsurface damage while protecting the first and second 0001 Si faces;

separating the first and second SiC seeds; and

thereafter attaching the unetched first 0001 Si face on the first SiC seed to a seed holder.

26. A method according to claim 25 wherein the step of etching a 0001 C face on each of the first and second SiC seeds to a depth sufficient to remove subsurface damage comprises etching to a depth greater than about 20 μm.

27. A method of protecting a 0001 Si face of a SiC seed during etching, the method comprising:

placing a first 0001 Si face on a first SiC seed sufficiently close to a second 0001 Si face on a second SiC seed to prevent etching of the first and second 0001 Si faces during a KOH etch of a first 0001 C face on the first SiC seed and a second 0001 C face on the second SiC seed; and

thereafter separating the unetched first and second 0001 Si faces.

28. A method according to claim 27 wherein the first 0001 Si face and the second 0001 Si face are placed directly against one another prior to the KOH etch.

29. A SiC seed with low density of 1c screw dislocations, basal plane, and threading dislocations on a growing surface, the seed comprising:

an unetched 0001 Si face that is flat to within about 10 μm; and

an etched 0001 C face having a 1c screw dislocation density of less than about 2000 cm^{-2}.

30. A SiC seed according to claim 29 further comprising a graphite seed holder attached to the unetched 0001 Si face.

31. A SiC seed structure comprising:

a first 0001 Si face on a first SiC seed directly against a second 0001 Si face on a second SiC seed.

32. A SiC seed structure according to claim 31 wherein gaps between the first and second 0001 Si faces on the first and second SiC seeds are less than about 10 μm.

33. A SiC seed structure according to claim 31 wherein gaps between the first and second 0001 Si faces on the first and second SiC seeds are less than about 5 μm.

Reduction Of 1c Screw Dislocations In The Production Of Bulk SiC Crystals

Abstract of the Disclosure

The invention is an improvement in a method of producing a high quality bulk single crystal of silicon carbide in a seeded sublimation system. The improvement includes etching the front face on each of a first and second SiC seed to a depth of greater than about 20 μm while protecting the opposite or back face on each of the first and second SiC seeds. Protection of the front faces occurs by placing the faces sufficiently close to one another to shield the back faces from being etched during etching of the respective unprotected front faces. Separation of the first and second SiC seeds occurs after the etching of the front faces is complete.

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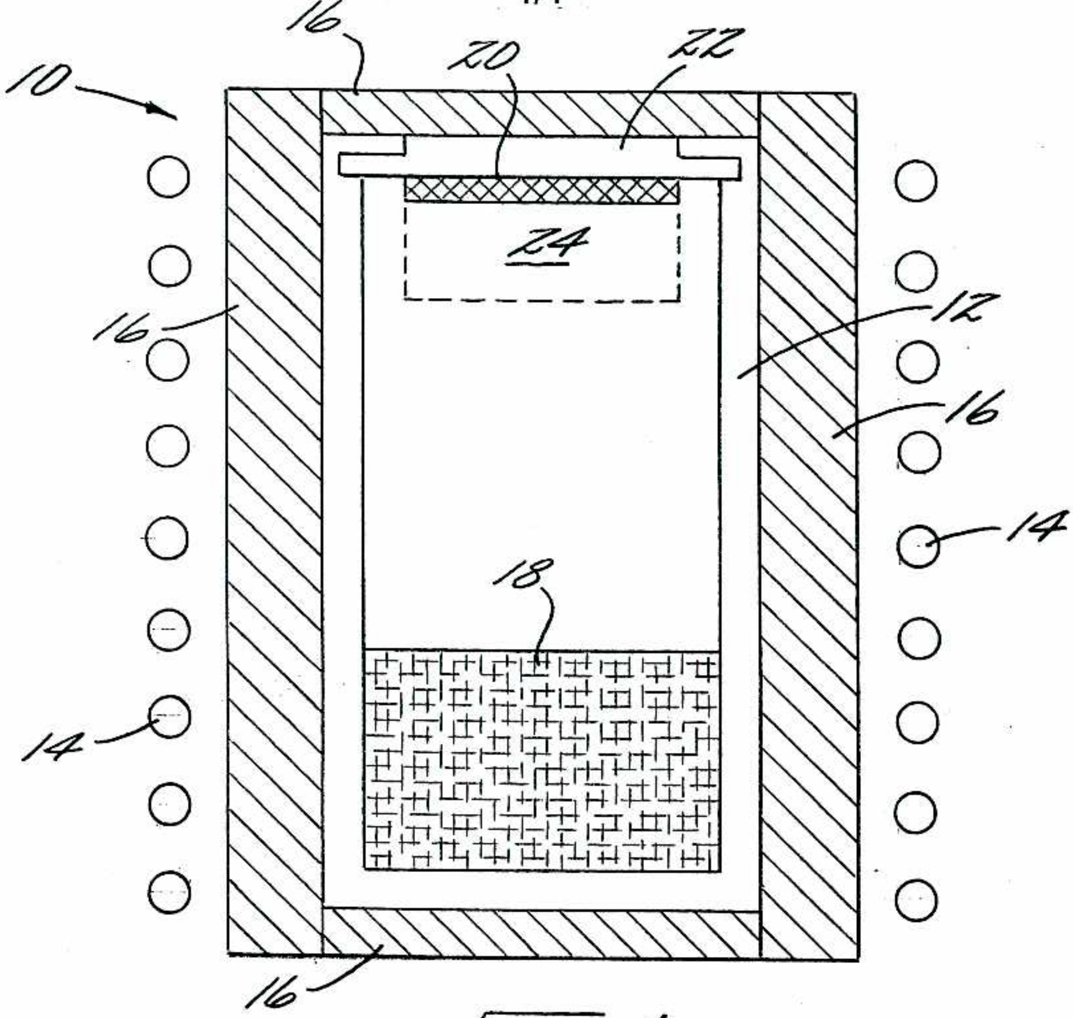

Fig. 1.

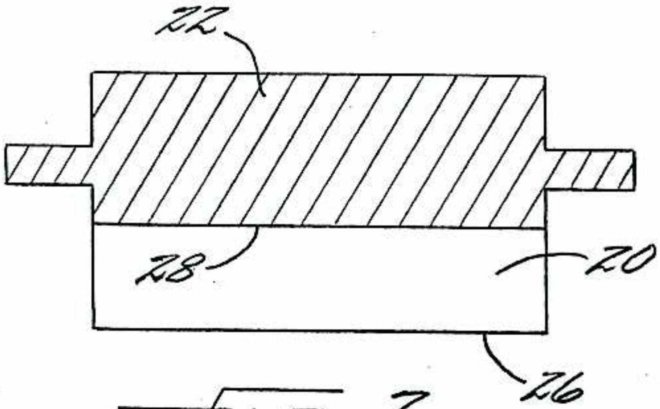

Fig. 2.

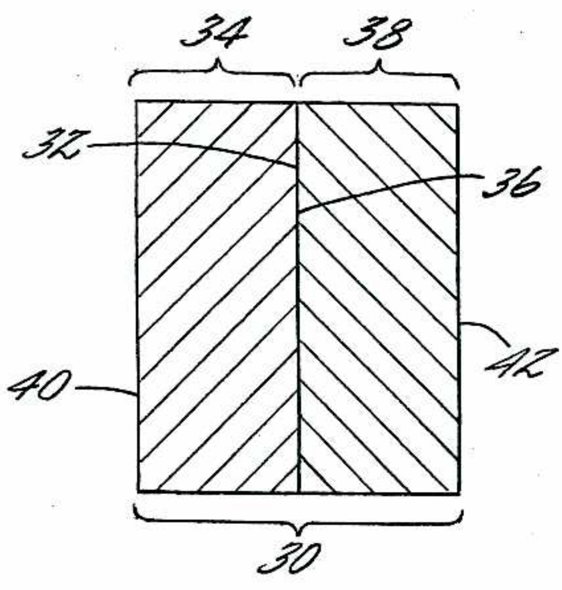

Fig. 3.

Attorney Docket No. 5308-526

HIGH POWER SILICON CARBIDE (SIC) PIN DIODES HAVING LOW FORWARD VOLTAGE DROPS

STATEMENT OF GOVERNMENT INTEREST

The present invention was developed with Government support under contract numbers N00014-02-C-D302, N00014-05-C-0202 and W911NF-04-2-0021. The Government has certain rights in this invention.

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and, more particularly, to PiN Diodes.

BACKGROUND OF THE INVENTION

In recent years, advances have been made in the development of silicon carbide (SiC) PiN diodes. For example, 4H-SiC PiN diodes may have the capability to block in excess of 20 kV while maintaining a low forward voltage (V_F) of 6.3 V at 3.2 A (100 A/cm^2) as discussed in LATEST ADVANCES IN 4H-SIC PIN AND MOS POWER DEVICES by M.K. Das (*Digest of International Semiconductor Device Research Symposium*, Washington, DC, 2003). However, these SiC PiN diodes suffer from an increase in V_F under forward bias as discussed in a paper by H. Lendenmann *et al*. (*Mater. Sci. Forum*, 353-356, 727 (2001). Furthermore, technological issues like, for example, effective edge termination, low resistivity p-type ohmic contacts, and forward voltage stability have historically hampered PiN diode development as discussed in, for example, papers by Crofton *et al*. (*Solid-State Electron.*, vol. 46, p. 689, 2002), H. Lendenmann *et al.* (*Mater. Sci. Forum*, Vol. 389-393 p. 1259, 2002) and J. Sumakeris, *et al. (Mater. Sci. Forum*, vol. 457-460, p. 1113, 2004).

SUMMARY OF THE INVENTION

Some embodiments of the present invention Silicon Carbide (SiC) PiN Diodes having a reverse blocking voltage (V_R) from about 3.0 kV to about 10.0 kV and a forward voltage (V_F) of less than about 4.3 V.

In further embodiments of the present invention, the PiN diodes may have an average forward current (I_F) of not greater than about 420A. In some embodiments of the present invention, the PiN diodes may have an average forward current (I_F) of not greater than about 200 A. In certain embodiments of the present invention, the PiN diode may be operating at a temperature of from about 25 °C to about 530 °C.

In still further embodiments of the present invention, the SiC PiN Diode may have a V_R of about 10.0 kV, an average I_F of about 50 A, a reverse leakage current (I_R) of about 0.5 mA, a V_F of about 3.8 V, a reverse recovery time (t_{rr}) of about 150 nsec and a reverse recovery charge (Q_{rr}) of about 1.1 µC when operating at a temperature of about 25 °C.

In some embodiments of the present invention, the SiC PiN Diode may have a blocking voltage (V_R) of about 10.0 kV, an average I_F of about 50 A, a reverse recovery time (t_{rr}) of about 300 nsec and a reverse recovery charge (Q_{rr}) of about 1.6 µC when operating at a temperature of about 150 °C.

In further embodiments of the present invention, the SiC PiN Diode may have a forward current of about 2 A. In these embodiments of the present invention, the SiC PiN Diode may be provided on a single chip, the chip being about 2.8 mm by 2.8 mm and the plurality of SiC PiN diodes may have a V_F of less than about 4.0 V, no less than about seventy percent of the plurality of SiC PiN diodes may have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and almost all of the plurality of SiC PiN diodes may have a forward voltage drift of no greater than 0.1V. The SiC PiN Diode may have a total yield of no less than about seventy percent.

In still further embodiments of the present invention, the SiC PiN Diode may have a forward current of about 5 A. In these embodiments of the present invention, a plurality of SiC PiN diodes may be provided on a single chip, the chip being about 2.8 mm by about 4.85 mm and the plurality of SiC PiN diodes may have a V_F of less than about 4.0 V, no less than about seventy one percent of the plurality of SiC PiN diodes may have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and no less than about ninety six percent of the plurality of

SiC PiN diodes may have a forward voltage drift of no greater than 0.1V. The SiC PiN Diode may have a total yield of no less than about sixty five percent.

In some embodiments of the present invention, the SiC PiN Diode may have forward current of about 25 A. In these embodiments of the present invention, a plurality of SiC PiN diodes may be provided on a single chip, the chip being about 5.4 mm by about 5.4 mm. The plurality of SiC PiN diodes may have a V_F of less than about 4.0 V, no less than about fifty percent of the plurality of SiC PiN diodes may have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and no less than about eighty seven percent of the plurality of SiC PiN diodes may have a forward voltage drift of no greater than 0.1V. The chip may have a total yield of no less than about forty three percent.

In further embodiments of the present invention, the SiC PiN Diode may have a forward current of about 50 A. In these embodiments of the present invention, the plurality of SiC PiN diodes may be provided on a single chip, the chip being about 8.65 mm by about 8.55 mm and the plurality of SiC PiN diodes may have a V_F of less than about 4.0 V, no less than about sixty five percent of the plurality of SiC PiN diodes may have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and no less than about ninety six percent of the plurality of SiC PiN diodes may have a forward voltage drift of no greater than 0.1V. The chip may have a total yield of no less than about sixty three percent.

In some embodiments of the present invention, the SiC PiN Diode may be a 4H SiC PiN Diode. The SiC PiN Diode may further include an n-type SiC substrate, an n-type SiC drift layer on the n-type SiC substrate and a p-type SiC Anode injection layer on the n-type drift layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-section illustrating PiN Diodes according to some embodiments of the present invention.

Figure 2 is a picture illustrating a 3" 4H-SiC wafers with 2A and 5A diodes, 25 A diodes and 50 A diodes from left to right according to some embodiments of the present invention.

Figure 3 is a graph illustrating reverse voltage (-V) vs. diode leakage current (A) of a 50 A diode (8.7 mm x 8.7 mm) and a 0.78 A diode according to some embodiments of the present invention.

Figure 4 is a graph illustrating forward diode current (A) vs. forward voltage (V) of a large 10 kV diode with a 3.75 forward drop at 50 A and 5.9 V forward drop at 328 A according to some embodiments of the present invention.

Figure 5 is a graph illustrating forward current (A) vs. forward voltage (V) measured at several temperatures according to some embodiments of the present invention.

Figure 6 is a graph illustrating a dI/dt reverse recovery transient showing fast turn-off with very little reverse recovery charge for a 10 kV, 20 A device, even at elevated temperatures according to some embodiments of the present invention.

Figure 7 is a graph illustrating voltage at 50 A/cm^2 (V) vs. Time (hr) showing that a novel epitaxy may produce more stable 4H-SiC PiN diodes (forward voltage stability) according to some embodiments of the present invention.

Figures 8A and 8B are graphs of number of devices vs. forward voltage drift (mV) for two different types of epitaxy according to some embodiments of the present invention.

Figure 9A and 9B are reverse blocking wafermaps for different types of epitaxy according to some embodiments of the present invention.

Figure 10 is a graph of time (hours) vs. current (μA) illustrating room temperature time dependent reverse leakage current at 5 kV reverse bias of six packaged 6 kV/25 A 4H-SiC PiN diodes according to some embodiments of the present invention.

Figure 11 is a graph of voltage (V) vs. current (A) temperature dependent forward I-V characteristics of Cree 4H-SiC 6 kV/50 A PiN diode (black) and Powerex 4.5 kV/60 A Si PiN diode (grey) according to some embodiments of the present invention.

Figure 12 is a graph of time (ns) vs. current (A) illustrating temperature dependent reverse recovery characteristics of Cree 4H-SiC 6 kV/50 A PiN diode and Powerex 4.5 kV/60 A Si PiN diode (circles) according to some embodiments of the present invention.

Figure 13 is a micoropipe distribution map for wafers on which 180 A/4.5 kV 4H-SiC PiN diodes were fabricated according to some embodiments of the present invention.

Figure 14 is a photograph illustrating a completed 4.5 kV 4H-SiC PiN diode wafer, with 180 Amp, 100 Amp, 13 Amp, and 0.2 Amp diodes according to some embodiments of the present invention.

Figures 15 is a graph illustrating forward characteristics of 180 Amp/4.5 kV 4H-SiC PiN diode according to some embodiments of the present invention.

Figure 16 is a graph illustrating reverse current-voltage characteristics of 180 Amp/4.5 kV 4H-SiC PiN diode according to some embodiments of the present invention.

Figure 17 is a graph illustrating pulsed forward current characteristics of a packaged 180 A (at 100 A/cm^2), 4.5 kV 4H-SiC PiN diode at 25°C according to some embodiments of the present invention.

Figure 18 is a graph illustrating reverse I-V characteristics of packaged 180 A, 4.5 kV 4H-SiC PiN diode at 25°C according to some embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. However, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. As used herein the term "and/or" includes any and all combinations of one or more of the associated listed items.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Like numbers refer to like elements throughout the specification.

It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another elements as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in the Figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", can therefore, encompass both an orientation of "lower" and "upper," depending of the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below. Furthermore, the term "outer" may be used to refer to a surface and/or layer that is farthest away from a substrate.

Embodiments of the present invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments of the present invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the present invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the present invention.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

It will also be appreciated by those of skill in the art that references to a structure or feature that is disposed "adjacent" another feature may have portions that overlap or underlie the adjacent feature.

Silicon carbide power devices based on 4H polytype silicon carbide (4H-SiC) according to some embodiments of the present invention have the potential to revolutionize the power semiconductor industry. Benefitting from an order of magnitude larger critical electric field than silicon (Si) and sufficiently high carrier mobility, 4H-SiC power devices may be designed with thinner, heavier doped drift layers, which may enable high voltage capability with low conduction and switching losses. The advantages of SiC are discussed in a paper by Singh *et al*. (*IEEE Trans. Electron Dev.*, vol. 49, p. 2054, 2002) the disclosure of which is hereby incorporated herein by reference in its entirety. Furthermore, the wide bandgap may enable high temperature operation well beyond the limits of conventional packaging. PiN diodes have been shown to operate at elevated temperatures up to 800 K as discussed in HIGH-TEMPERATURE (UP TO 773K) OPERATION OF 6-KV 4H-SIC JUNCTION DIODES to Levinshtein, *et al.* (Solid-State Electronics; July 2005, Vol. 49 Issue 7, pages 1228-1232, the disclosure of which is hereby incorporated herein by reference as if set forth in its entirety. 4H-SiC Schottky diodes are supplanting Si in

300 V – 1200 V applications. For even higher voltage applications, the rectifier of choice appears to be the 4H-SiC PiN diode, which has been demonstrated to block up to 20 kV with low V_F of 6 V as discussed in LATEST ADVANCES IN 4H-SIC PIN AND MOS POWER DEVICES by Das (*Digest of International Semiconductor Device Research Symposium*, Washington, DC, 2003, the disclosure of which is incorporated herein by reference as if set forth in its entirety.

However, as discussed above, technological issues like effective edge termination, low resistivity p-type ohmic contacts, and forward voltage stability have historically hampered PiN diode development. Thus, some embodiments of the present invention provide from 6 kV to about 10 kV, up to 50 A, 4H-SiC PiN diodes that may not expericence the problems of existing SiC PiN diodes. In particular, high power 10 kV, up to 50 A, SiC PiN diodes having a low forward voltage drop (V_F) of 3.75 V and a fast reverse recovery time of 150 nsec are provided according to some embodiments of the present invention.

Furthermore, SiC PiN diodes according to some embodiments of the present invention may not experience the historical problems with the SiC PiN diode technology, such as ineffective edge termination (V_{BD} increased to > 70% of ideal breakdown voltage), poor ohmic contacts to p-type SiC (ρ_C reduced to < 10^{-4} Ωcm^2), and forward voltage drift (ΔV_F reduced to < 0.1 V). Some embodiments of the present invention have addressed these issues with design, material, and process improvements which have resulted in high overall device yields according to some embodiments of the present invention as will be discussed further below with respect to Figures 1 through 18.

Exemplary devices according to some embodiments of the present invention are schematically illustrated in Figure 1. However, embodiments of the present invention should not be construed as limited to the particular exemplary embodiments described herein but may include any suitable structure that provides PiN Diode characteristics as described herein.

Referring first to Figure 1, a cross section of PiN diodes, for example, a 10 kV, 4H-SiC PiN diode, according to some embodiments of the present invention will be discussed. As illustrated in Figure 1, a substrate 100 is provided on which PiN Diodes according to some embodiments of the present invention may be formed. In particular embodiments of the present invention, the substrate 100 may be a conducting n-type silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide. The substrate 100 may have a resistivity of from about 0.017 to about 0.022. An n-type drift layer 110 is provided on the substrate 100. The n-type drift layer may have a thickness of about 100 μm and a carrier concentration of about 2 X $10^{14}cm^{3}$. A p-type anode injection layer 127 is provided on the drift layer 110. The p-type anode injection layer 127 may have a thickness of about 2.5 μm and a carrier concentration of about 8 X $10^{18}cm^{3}$. The p-type anode injection layer 127 may be doped with aluminum (Al). The p-type anode injection layer 127 may have first and second portions. A first portion may be a p^{+} layer having a carrier concentration of about 8 X $10^{18}cm^{3}$. A second layer may be provided on the first layer. The second layer may be a p^{++} layer having a carrier concentration of 5 X $10^{20}cm^{3}$.

The n-type drift layer 110 and the p-type anode injection layer 127 may be epitaxial layers that are continuously grown on the substrate, for example, a 0.6 cm^{-2} micropipe density 8° off-axis (0001) 4HN 3 inch substrate 100. The epitaxial layers may be fabricated using, for example, the process described in United States Patent Publication No. US 2005/0064723 to Sumakeris, the disclosure of which is hereby incorporated by reference as if set forth in its entirety. Other low BPD epitaxial processes discussed in, for example, a paper by Sumakeris *et al.* (*Mater. Sci. Forum*, 457-460, 1113 (2004)) and Sumakeris *et al*. (*ICSCRM* 2005, Pittsburgh, PA (2005)) the disclosures of which are hereby incorporated herein by reference in their entirety.

The device is mesa isolated by etching down to the n^{-} drift layer 110 in the field areas using, for example, a reactive ion etch (RIE). Mesa areas for each diode design were based on a designed current density of 100 A/cm^2 for 2 A, 5 A, and 50 A diodes, or 142 A/cm2 for 25 A diodes, with mesas measuring 1.46 mm x 1.46 mm (2 A), 1.46 mm x 3.51 mm (5 A), 4.21 mm x 4.21 mm (25 A), and 7.08 mm x 7.08 mm (50A).

It will be understood that the mesa sizes discussed herein are provided for exemplary purposes and embodiments of the present invention are not limited to this configuration. For example, the mesa sizes discussed above may only correspond to 6 kV diodes according to some embodiments of the present invention. It will be further understood that mesa sizes may vary slightly for different blocking thicknesses. Thus, for example, a mesa for a 50A/10kV diode may have slightly different dimensions than a mesa for a 50A/6kV diode.

An aluminium (Al) implanted guard ring-based termination 115 is provided/formed around the device periphery while a nitrogen (N) implanted channel stop regions 125 ground the field area away from the devices. The implants are activated with a 1600-1650°C Argon (Ar) anneal in the presence of silicon (Si) overpressure.

In some embodiments of the present invention, a junction termination extension (JTE) technique may be used as discussed in *Multiple-Zone Single-Mask Junction Termination Extension: A High-Yield Near-Ideal Breakdown Voltage Technology* by Trantraporn *et al.* (*IEEE TRATISACTIONS ON ELECTRON DEVICES*, Vol. ED-34, No. 10, OCTOBER 1987), the disclosure of which is incorporated herein by reference as if set forth in its entirety.

A passivation layer 120 is provided on the surface of the device. The passivation layer 120 may be formed using a two step passivation process. A first portion of the passivation layer 120 is thermally grown to a thickness of from about 600 Å to about 700 Å. A second portion of the passivation layer 120 may be provided on the first portion. The second portion may be deposited on the first portion using, for example, a chemical vapor deposition (CVD) process at a temperature of about 410 °C. The second portion may have a thickness of about 1 µm. The passivation layer 120 may include silicon dioxide (SiO_2) and/or polymide. An ohmic contact 131 including, for example, titanium/aluminium (Ti-Al) is provided on the anode injection layer 127. An ohmic contact 130 including, for example, nickel (Ni) is provided on the cathode. The contacts were annealed at 1000°C in Ar. As used herein the term "ohmic contact" refers to contacts where an impedance associated therewith is substantially given by the relationship of Impedance = V/I, where V is a voltage across the contact and I is the current, at substantially all expected operating frequencies (*i.e.,* the impedance associated with the ohmic contact is substantially the same at all operating frequencies) and currents. Gold (Au) overlayers 140 and 141 are provided on the ohmic contacts 130 and 131, respectively, to aid in current spreading and/or die attach. In other words, sintered Ti-Al and Ni contacts 130 and 131 are made to the anode and cathode, respectively, before depositing thick Au overlayers 140 and 141.

PiN Diodes according to some embodiments of the present invention, for example, 50A PiN diodes, may be provided on 8.7 mm x 8.7 mm chips, which have a

0.50 cm^2 active area. In some embodiments of the present invention, a total of 48 chips can be fabricated on a single 3 inch wafer as illustrated, for example, in Figure 2. In particular, Figure 2 illustrates completed wafers with, from left to right, 2 A and 5 A diodes (combined on one wafer), 25 A diodes, and 50 A diodes.

Referring now to Figure 3, a graph illustrating Reverse Voltage (-V) vs. Diode Leakage Current (A) of a 50 A diode (8.7 mm x 8.7 mm) and a 0.78 A diode according to some embodiments of the present invention will be discussed. Figure 3 illustrates the reverse blocking capability of a typical PiN diode. Reverse blocking is measured out to 9 kV where the leakage current exceeds the current compliance limit of the measurement apparatus. Extrapolating the leakage current to 10 kV a low leakage current density of approximately 1 mA/cm^2 (based on a device footprint of 0.615 cm^2) is estimated. The validity of this extrapolation is contingent on the absence of avalanching prior to 10 kV. Reverse operation of small 0.78 A diodes confirm full 10 kV blocking capability without any premature avalanche as illustrated in Figure 3. Hence, a 10 kV blocking capability is implied for the large devices blocking, such as greater than 7 kV. As illustrated in Figure 3, the large diode demonstrates greater than 9 kV blocking that is current compliance limited. The dashed line extrapolates the reverse blocking to 10 kV with only 1 mA/cm^2. The small diode confirms 10 kV capability.

Referring now to Figure 4, pulsed forward I-V characteristic of a large 10 kV diode with a 3.75 V forward drop at 50 A and 5.9 V forward drop at 328 A indicating a high level of conductivity modulation. As illustrated in Figure 4, a low forward voltage drop of 3.75 V is observed at 50 A (100 A/cm^2) indicating a high degree of conductivity modulation. 4H-SiC PiN diodes are capable of handling very high current densities and we have measured this large device out to a pulsed current of 328 A (656 A/cm^2) at a low forward drop of 5.9 V. For a single chip, this demonstrates over 3 MW of pulsed power. As illustrated in Figure 5, these devices also show excellent forward characteristics with respect to temperature.

Referring now to Figure 5, forward I-V curve measured at several temperatures on a small 10 kV device where a positive temperature coefficient at high current density facilitates device paralleling. The differential resistance at low current density remains constant versus temperature because the increase in carrier lifetime is balanced by the reduction in carrier mobility and diffusivity. The V_F at low current densities decreases slightly with temperature due to bandgap narrowing effects that reduce the built-in potential. This introduces a concern for thermal runaway. However, at high current densities, the behavior reverses to a positive temperature coefficient, thereby making these devices attractive for use in a parallel configuration.

Referring now to Figure 6, a graph illustrating a dI/dt reverse recovery transient showing fast turn-off with very little reverse recovery charge for a 10 kV, 20 A device, even at elevated temperatures according to some embodiments of the present invention will be discussed. Large dI/dt reverse recovery transient showed fast turn-off with very little reverse recovery charge for a 10 kV, 20 A device, even at elevated temperatures. One potential drawback of a well modulated PiN diode is that the switching ability may suffer, especially the turn-off transient, due to the extra time needed for carrier removal in the drift layer. As illustrated in Figure 6, the reverse recovery of the 10 kV diodes shows a fast 150 nsec recovery at room temperature with very little reverse recovery charge despite an aggressive dI/dt of 330 A/μsec. At elevated temperatures, the high speed switching capability remains intact with very minimal charge increase and a 300 nsec recovery time.

To be a commercially viable product, stable device performance should be demonstrated across the entire wafer. Historically, the 4H-SiC PiN diodes have suffered from forward voltage instability, where the V_F may increase by several volts during forward operation as discussed in H. Lendenmann *et al.* (*Mater. Sci. Forum*, Vol. 389-393 p. 1259, 2002), the disclosure of which is incorporated herein by reference as if set forth in its entirety. As discussed in Sumakeris, *et al.* (*Mater. Sci. Forum*, vol. 457-460, p. 1113, 2004), under forward bias, bipolar current flow in the "i" layer causes electron-hole recombination; the recombination provides energy to the lattice allowing basal plane screw dislocations (BPD) to generate stacking faults; the stacking fault becomes negatively charged by trapping electrons; electron injection is attenuated at the cathode with a corresponding reduction of hole injection at the anode; the area under the fault becomes devoid of plasma thereby reducing the effective current handling area of the device; and a larger amount of forward bias is now needed to maintain the same forward current level.

Hence, the key to producing drift-free PiN structures is the reduction of BPDs. Typically, the areal density of BPDs in the substrate is ~2000 cm^{-2} of which 90% can be turned into relatively benign threading edge dislocations in epitaxy. Recent innovations have reduced the epilayer BPD density below 10 cm^{-2} as discussed in Sumakeris, *et al.* (*Mater. Sci. Forum*, vol. 457-460, p. 1113, 2004) such that the devices have become fairly well behaved as illustrated in Figure 7. Devices can now be effectively screened for their V_F stability by a simple on-wafer 30 min constant current stress at 50 A/cm^2 as discussed in B.A. Hull *et al.* (*J Electron. Mater.*, vol. 34, no. 4, 2005), the disclosure of which is hereby incorporated herein by reference as if set forth in its entirety.

Referring now to Figures 8A and 8B, graphs of number of devices vs. forward voltage drift (mV) for two different types of epitaxy according to some embodiments of the present invention will be discussed. The histograms of Figures 8A and 8B illustrate the number of stable devices by binning the devices according to the amount of forward voltage increase after the forward stress. Using 100 mV as an acceptable amount of V_F drift, we observe that the drift yield increased from 17% to 67% by incorporating the novel epitaxy while not compromising the reverse blocking yield as illustrated in Figures 9A and 9B. Figures 9A and 9B are reverse blocking wafermaps for different types of epitaxy according to some embodiments of the present invention.

Epitaxy	BPD (cm^{-2})	Device	Drift Yield	10 kV Yield	Total Yield
Original Process	180	50 A	17 %	37 %	6 %
New Process	**20**	**50 A**	**67 %**	**35 %**	**23 %**

TABLE 1

Table 1 illustrates progress toward making the large hero devices more prevalent across the wafer. Overall device yield is a respectable 23% for 10 kV 50 A PiN diodes having improved by nearly 4x over the previous technology.

Thus, as discussed herein, according to some embodiments of the present invention, state-of-the-art 10 kV, 50 A 4H-SiC diodes have been fabricated with low V_F of 3.75 V, fast switching, and stable operation with respect to temperature.

Characteristic	Symbol	Units	Cree SiC	Pwrex Si	VMI UF Si
25°C Peak Reverse Blocking	V_{RRM}	kV	10	9.0	10
25°C Reverse Leakage Current at V_{RRM}	I_{RRM}	mA	0.5	1.0	0.1
25°C Average Forward Current	$I_{F(av)}$	Amps	50	60	50
25°C Forward Voltage at $I_{F(av)}$	**V_F**	**Volts**	**3.8**	**12.4**	**14.0**
25°C Reverse Recovery Time	t_{rr}	nsec	150	230	100
25°C Reverse Recovery Charge	**Q_{rr}**	**μC**	**1.1**	**11**	**5**
150°C Reverse Recovery Time	HT t_{rr}	nsec	300	-	500
150°C Reverse Recovery Charge	**HT Q_{rr}**	**μC**	**1.6**	**-**	**24.75**

TABLE 2

Table 2 illustrates how the 4H-SiC PiN diodes compare with similarly rated Si rectifier stacks. In addition to the simplicity of a single chip, the 4H-SiC PiN diode offers a lower forward voltage drop, reduced reverse recovery charge, and excellent high temperature characteristics where the switching is well behaved and the on-current does not require additional derating. With the advent of >20% overall device yield, a significant step has been made in the evolution of a commerically viable SiC PiN diode technology expected to meet the demands of high voltage, high frequency power conversion applications.

In some embodiments of the present invention the epitaxial layers may be formed as discussed in EVOLUTION OF DRIFT-FREE, HIGH POWER 4H-SIC PIN DIODES to Das *et al*. (*ICSCRM* 2005, Pittsburg, PA, 2005), the disclosure of which is hereby incorporated herein by reference as if set forth in its entirety.

Results according to further embodiments of the present invention will now be discussed with respect to Figures 10 through 12. Table 3 summarizes the wafer-level yield statistics for the best yielding wafers of various current rated PiN diodes that are designed to block 6kV according to some embodiments of the present invention. As illustrated in Table 3, the best total wafer yield of 69 percent was achieved on 2A diodes. Nevertheless, even on a 50 A diode wafer, with a die size of 8.64 mm x 8.56 mm, a total yield of 62 percent was achieved. The best total yield achieved on a 25 A wafer was somewhat lower, at 43 percent, but the 25 A diode wafers were fabricated with previous generation epitaxial growth and device fabrication processes. The latest results from the 2 A/5 A and 50 A diode designs, wafer-level device yields that indicate the commercial viability of the 4H-SiC PiN diode technology have been achieved.

Diode Rating	Chip dimensions [mm]	V_F Yield [$V_F \leq 4.0$ V]	6 kV Blocking Yield [$I_R \leq 1$ mA/cm^2]	V_F Drift Yield [$\Delta V_F \leq 0.1$ V]	Total Yield
2 A	2.79 x 2.79	100%	70.6%	98.3%	69.4%
5 A	2.79 x 4.84	100%	71.4%	95.7%	64.7%
*25 A	5.36 x 5.36	100%	49.0%	87.1%	42.7%
50 A	8.64 x 8.56	100%	64.4%	96.6%	62.2%

* 25 Amp diode wafer was from an earlier generation process

TABLE 3

Referring now to Figure 10, time dependent leakage current of six packaged 6 kV/25 A 4H-SiC PiN diodes under long term reverse bias at 5 kV will be discussed. As illustrated therein, during 900 hours at 5 kV reverse bias, the maximum increase in leakage current for any diode was 6 μA. However, some arcing between package leads was observed during testing (especially with increases in humidity) and no effort to separate diode leakage currents from package leakage currents were made. Thus, reverse leakage current increases could not be attributed to the diodes themselves. No change in the forward I-V characteristics were observed following long-term reverse biasing.

Referring now to Figure 11, the temperature dependent forward current-voltage (I-V) characteristics of a 50 A 4H-SiC PiN diode along with those of a 4.5 kV/60 A Si PiN diode will be discussed. The 4H-SiC PiN diode was taken to 60 A (120 A/cm^2) to provide a suitable comparison to the Si PiN diode. At 60 A, the V_F of the SiC diode was 0.75 V lower than the Si diode at room temperature, corresponding to a 45 W decrease in DC forward dissipated power, or a reduction of 18 percent. At 150°C, the 4H-SiC PiN diode reduced the power dissipation by 32 W at 60 A, or 14 percent, from that of the Si PiN diode.

Referring now to Figure 12, a comparison of the reverse recovery transients at 25°C and 150°C of the 4H-SiC PiN diode and the Si PiN diode will be discussed. Furthermore, peak reverse recovery current (I_{RM}), reverse recovery time (t_{rr}), stored charge (Q_{rr}), and stored energy (E_{rr}) are presented in Table 4 for all conditions tested.

	Peak Reverse Current, I_{RM} [Amps]		Reverse Recovery Time, t_{rr} [nsec]		Stored Charge, Q_{rr} [μC]		Stored Energy, E_{rr} [mJ]	
	4H-SiC	Si	4H-SiC	Si	4H-SiC	Si	4H-SiC	Si
25°C	39.8	54.8	270	360	6.3	11.7	1.8	3.2
50°C	43.3	56.6	300	375	7.7	12.7	2.2	3.5
100°C	52.1	60.1	360	430	11.2	15.8	3.1	4.4
150°C	61.5	66.3	440	490	15.7	19.1	4.3	5.4

TABLE 4

The diodes were switched from a nominal 50 A DC forward current to -500 V reverse bias at a 300 A/μs switching transient. At all temperatures the 4H-SiC PiN diode showed significantly lower I_{RM}, t_{rr}, Q_{rr}, and Err than the Si PiN diode. Based on measured Err, switching loss power savings for the 4H-SiC PiN diode range from 20 percent at 150°C to 44 percent at 25°C. Due to the need for separating the diode (at temperature) from the test switch (at room temperature), parasitic inductance and resistance in the circuit wires may be artificially skewing the reverse recovery characteristics to longer recovery times and higher energies. However, no alterations to the test circuit were made between testing the 4H-SiC diode and the Si diode, thus providing an accurate comparison. Reverse recovery switching bias was limited to a 500 V reverse bias by limitations in test equipment.

Results according to further embodiments of the present invention will now be discussed with respect to Figures 13 through 16. A 4H-SiC PiN diode that blocks up to about 4.5 kV and conducts up to about 180 A (at 100A/cm2) under a low forward voltage (VF) of 3.5 V is provided. This single-chip 4H-SiC PiN diode, at 1.5 cm x 1.5 cm, is the largest discrete 4H-SiC power device ever reported, with over 2 times the area of the previous largest chip, a 1 cm x 1 cm, 100 A 4H-SiC thyristor as discussed in Agarwal *et al*. (ICSCRM 2005, Pittsburgh, PA, (Sept. 2005)), the disclosure of which is incorporated herein by reference as if set forth in its entirety. The diode exhibited a leakage current of less than about 5.0 μA at 4.5 kV, or less than 2.8 $\mu A/cm^2$, giving a rated forward current to reverse leakage current ratio of greater than about 3 x 107. Successful fabrication of such a large discrete 4H-SiC PiN diode with such exceptional breakdown characteristics is a testament to the advances in SiC materials and device fabrication technologies.

The 180 A/4.5 kV 4H-SiC PiN diodes were fabricated on 3 inch 4H-SiC wafers cut 8° off of the [0001] basal plane. A exemplary micropipe map of the wafers is illustrated in Figure 13. The wafers had an overall micropipe density of 0.2 micropipes/cm^2, with a total of 10 micropipes on wafer, which to date is one of the best micropipe densities achieved in any 3 inch 4H-SiC boule ever grown at Cree as discussed in Powell (Industrial News Session, ICSCRM 2005, Pittsburgh, PA, (Sept. 2005)), the disclosure of which is incorporated herein by reference as if set forth in its entirety. Furthermore, all but one of the micropipes were located near the wafer periphery for an effective micropipe density of 0.03/cm^2 over the central 70% of the wafer area. A N-doped 50 μm thick epitaxial layer doped 2.0 x 10^{14} cm^{-3} and an Al doped 2.5 μm thick epitaxial layer doped at 8.0 x 10^{18} cm^{-3} were grown continuously in one epitaxial run. An epitaxial process that reduces the density of screw-type [0001] basal plane dislocations (BPD) in the epitaxial film to suppress the irreversible increase in VF (VF drift) typically seen in 4H-SiC PiN diodes was used. Such an epitaxial process is discussed in, for example, Sumakeris, *et al.* (*Mater. Sci. Forum*, vol. 457-460, p. 1113, 2004), the disclosure of which is incorporated herein by reference as if set forth in its entirety. Diode mesas measuring 13.58 mm per side (180 A diodes) or 10.01 mm per side (100 A diodes) were isolated with a reactive ion etch.

A p-type multi-zone junction termination extension (JTE) was then ion implanted around the mesa peripheries, followed by an n-type channel stop around the chip peripheries. Following implant activation at 1650°C, the diodes were passivated with a 1.0 μm SiO_2 layer, and ohmic contacts were deposited on the anode and cathode and were annealed at 1000°C in Argon. Finally thick Au layers were deposited on the anode and cathode contacts for current spreading and die-attach.

A photograph of a completed wafer is illustrated in Figure 13. Furthermore, Figures 14 and 15 illustrate on-wafer diode forward and the optimum reverse I-V characteristics of a 180 A diode. The V_F at 180 A was 3.5 V, and the reverse leakage current at 4.5 kV was 2.0 μA, or 1.1 μA/cm2. There was a sharp increase in the reverse leakage current near 4.5 kV, showing well behaved avalanche breakdown characteristics. On the best wafer (of two), five of the six 180 A diodes reached the blocking specification of less than 900 μA (0.5 mA/cm2) at 4.5 kV, and the overall lot yield was 8 diodes of 12. This phenomenal single wafer device yield of 83% (or 67% total lot yield) demonstrates that extremely high power, discrete SiC devices are commercially feasible with current state of the art 4H-SiC substrates, epitaxy, and device processing.

Results according to further embodiments of the present invention will now be discussed with respect to Figures 17 through 18. Figure 17 is a graph illustrating pulsed forward current characteristics of a packaged 180 A (at 100 A/cm^2), 4.5 kV 4H-SiC PiN diode at 25°C and a maximum pulsed current of 420 Amps at 3.36 Volts forward bias. Furthermore, Figure 18 is a graph illustrating Reverse I-V characteristics of a packaged 180 A, 4.5 kV 4H-SiC PiN diode at 25°C.

In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation.

THAT WHICH IS CLAIMED IS:

1. A Silicon Carbide (SiC) PiN Diode having a reverse blocking voltage (V_R) from about 3.0 kV to about 10.0 kV and a forward voltage (V_F) of less than about 4.3 V.

2. The SiC PiN Diode of Claim 1 having an average forward current (I_F) of not greater than about 420 A.

3. The SiC PiN Diode of Claim 2 having an average forward current (I_F) of not greater than about 200 A.

4. The SiC PiN Diode of Claim 2 operating at a temperature of from about 25 °C to about 530 °C.

5. The SiC PiN Diode of Claim 4 having a V_R of about 10.0 kV, an average I_F of about 50 A, a reverse leakage current (I_R) of about 0.5 mA, a V_F of about 3.8 V, a reverse recovery time (t_{rr}) of about 150 nsec and a reverse recovery charge (Q_{rr}) of about 1.1 μC when operating at a temperature of about 25 °C.

6. The SiC PiN Diode of Claim 4 having a blocking voltage (V_R) of about 10.0 kV, an average I_F of about 50 A, a reverse recovery time (t_{rr}) of about 300 nsec and a reverse recovery charge (Q_{rr}) of about 1.6 μC when operating at a temperature of about 150 °C.

7. The SiC PiN Diode of Claim 1 having a forward current of about 2 A:

wherein a plurality of SiC PiN diodes are provided on a single chip, the chip being about 2.8 mm by 2.8 mm;

wherein the plurality of SiC PiN diodes have a V_F of less than about 4.0 V, no less than about seventy percent of the plurality of SiC PiN diodes have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and almost all of the plurality of SiC PiN diodes have a forward voltage drift of no greater than 0.1V.

8. The SiC PiN Diode of Claim 7, wherein the chip has a total yield of no less than about seventy percent.

9. The SiC PiN Diode of Claim 1 having a forward current of about 5 A:

wherein a plurality of SiC PiN diodes are provided on a single chip, the chip being about 2.8 mm by about 4.85 mm;

wherein the plurality of SiC PiN diodes have a V_F of less than about 4.0 V, no less than about seventy one percent of the plurality of SiC PiN diodes have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and no less than about ninety six percent of the plurality of SiC PiN diodes have a forward voltage drift of no greater than 0.1V.

10. The SiC PiN Diode of Claim 9, wherein the chip has a total yield of no less than about sixty five percent.

11. The SiC PiN Diode of Claim 1 having a forward current of about 25 A:

wherein a plurality of SiC PiN diodes are provided on a single chip, the chip being about 5.4 mm by about 5.4 mm;

wherein the plurality of SiC PiN diodes have a V_F of less than about 4.0 V, no less than about fifty percent of the plurality of SiC PiN diodes have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0 mA/cm^2 and no less than about eighty seven percent of the plurality of SiC PiN diodes have a forward voltage drift of no greater than 0.1V.

12. The SiC PiN Diode of Claim 11, wherein the chip has a total yield of no less than about forty three percent.

13. The SiC PiN Diode of Claim 1 having a forward current of about 5 A:

wherein a plurality of SiC PiN diodes are provided on a single chip, the chip being about 8.65 mm by about 8.55 mm;

wherein the plurality of SiC PiN diodes have a V_F of less than about 4.0 V, no less than about sixty five percent of the plurality of SiC PiN diodes have a blocking voltage of about 6kV and a reverse leakage current (I_R) of not greater than 1.0

mA/cm^2 and no less than about ninety six percent of the plurality of SiC PiN diodes have a forward voltage drift of no greater than 0.1V.

14. The SiC PiN Diode of Claim 13, wherein the chip has a total yield of no less than about sixty three percent.

15. The SiC PiN Diode of Claim 1, wherein the SiC PiN Diode comprises a 4H SiC PiN Diode.

16. The SiC PiN Diode of Claim 15, wherein the SiC PiN Diode further comprises:

an n-type SiC substrate;

an n-type SiC drift layer on the n-type SiC substrate; and

a p-type SiC Anode injection layer on the n-type drift layer.

17. A 4H Silicon Carbide (SiC) PiN Diode having a reverse blocking voltage (V_R) from about 3.0 kV to about 10.0 kV and a forward voltage (V_F) of less than about 4.3 V, an average forward current of not greater than about 420 A and operating at a temperature of from about 25 °C and about 530 °C.

18. The SiC PiN Diode of Claim 17, wherein the SiC PiN Diode further comprises:

an n-type SiC substrate;

an n-type SiC drift layer on the n-type SiC substrate; and

a p-type SiC Anode injection layer on the n-type drift layer.

19. A PiN Diode having a reverse blocking voltage (V_R) of about 10.0 kV, a forward current of no greater than about 50 A and a forward voltage (V_F) of less than about 3.8 V.

20. The PiN Diode of Claim 19 having a reverse recovery charge of less than 5.0 μC when operating at a temperature of 25 °C.

21. The PiN Diode of Claim 20, wherein the reverse recovery charge is less than 2.0 μC when operating at a temperature of 25 °C.

22. The PiN Diode of Claim 21, wherein the PiN Diode comprises a 4H silicon carbide (SiC) diode.

23. The PiN Diode of Claim 19 having a reverse recovery charge of less than 24.0 μC when operating at a temperature of 150 °C.

24. The PiN Diode of Claim 23, wherein the reverse recover charge is less than 2.0 μC when operating at a temperature of 150 °C.

25. The PiN Diode of Claim 24, wherein the PiN Diode comprises a 4H silicon carbide (SiC) diode.

HIGH POWER SILICON CARBIDE (SIC) PIN DIODES HAVING LOW FORWARD VOLTAGE DROPS

ABSTRACT OF THE DISCLOSURE

Silicon Carbide (SiC) PiN Diodes are provided having a reverse blocking voltage (V_R) from about 3.0 kV to about 10.0 kV and a forward voltage (V_F) of less than about 4.3 V.

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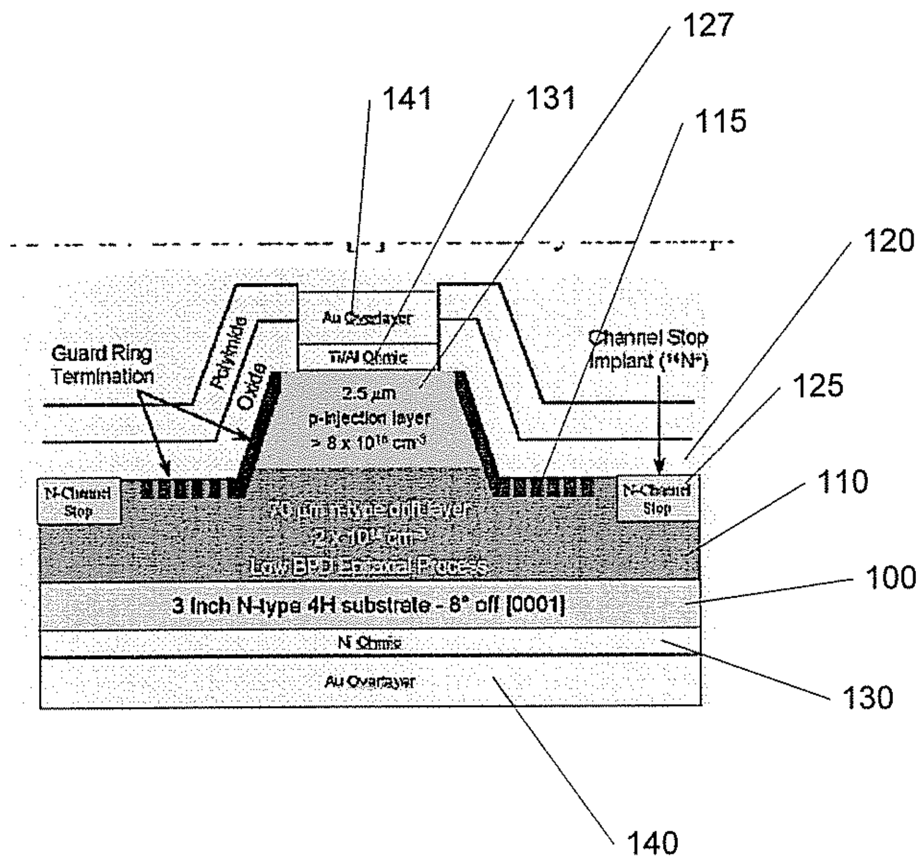

Figure 1

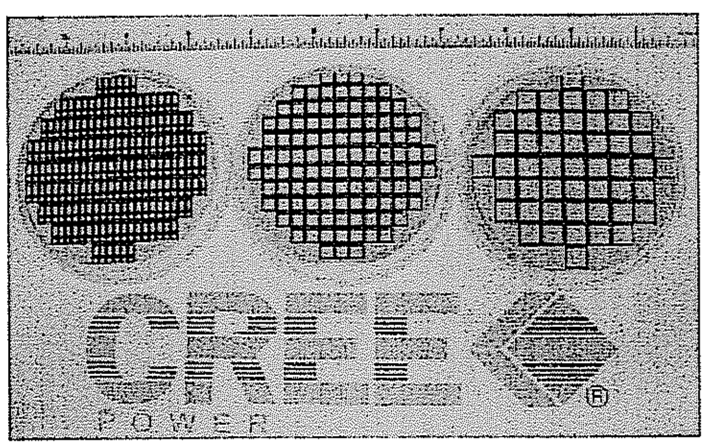

Figure 2

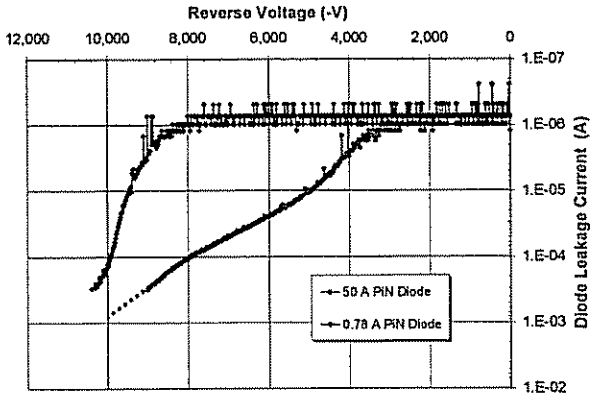

Figure 3

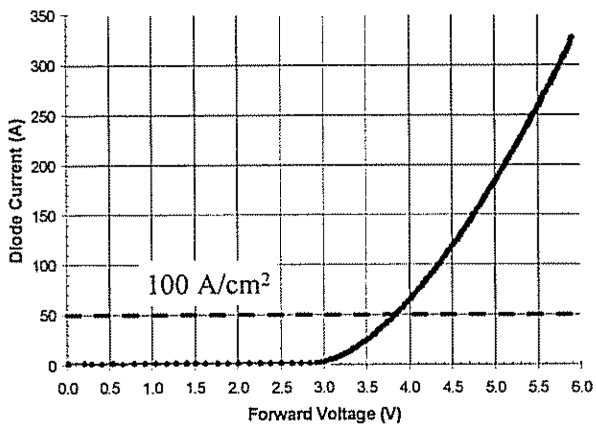

Figure 4

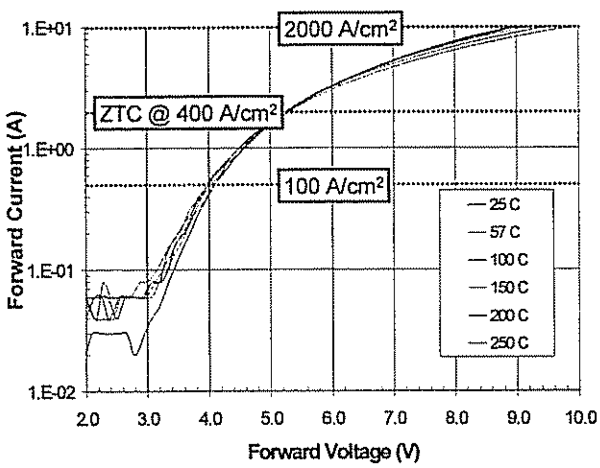

Figure 5

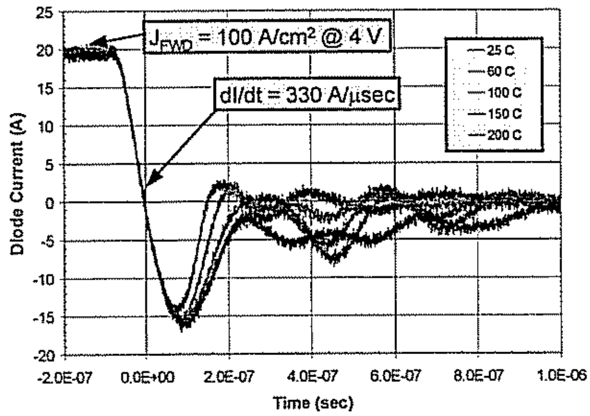

Figure 6

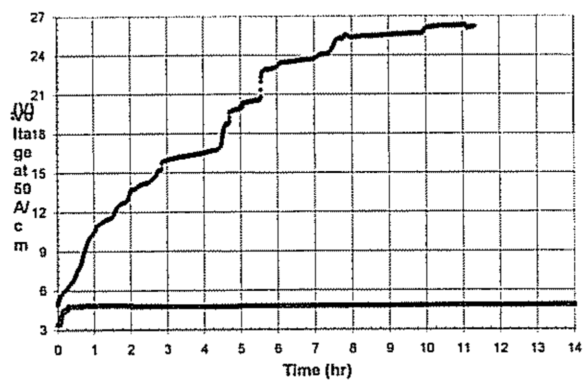

Figure 7

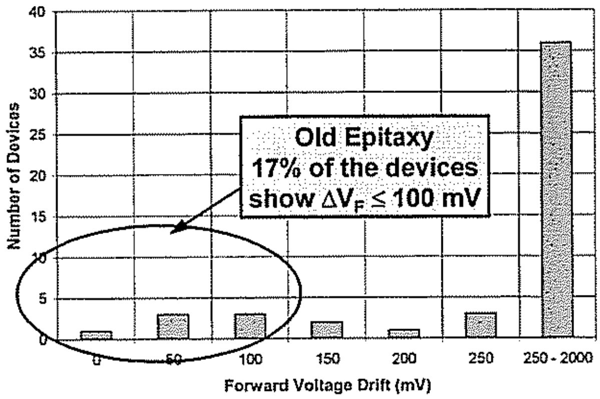

Figure
8A

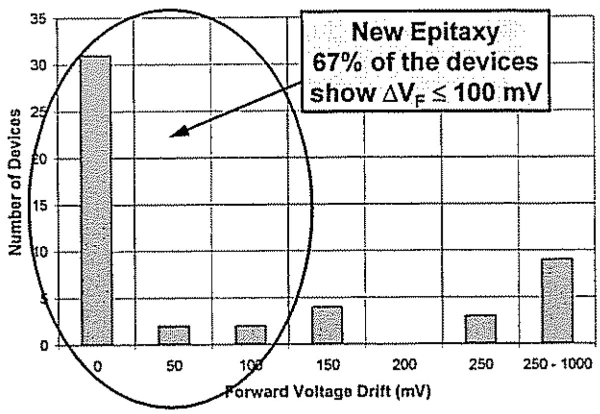

Figure
8B

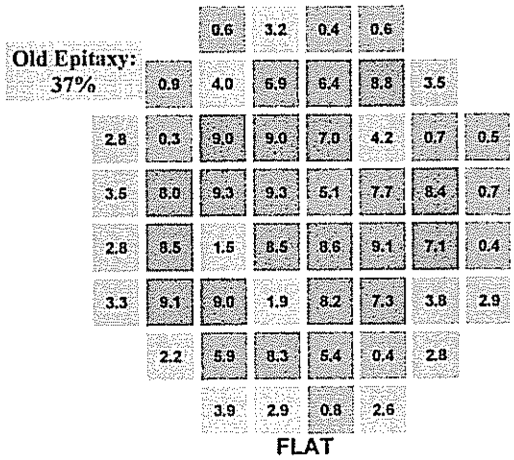

Figure
9A

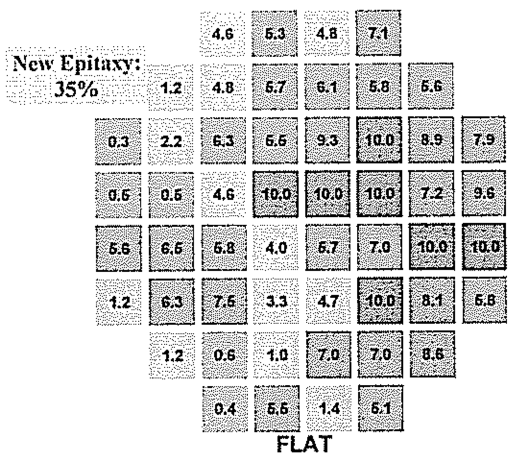

Figure
9B

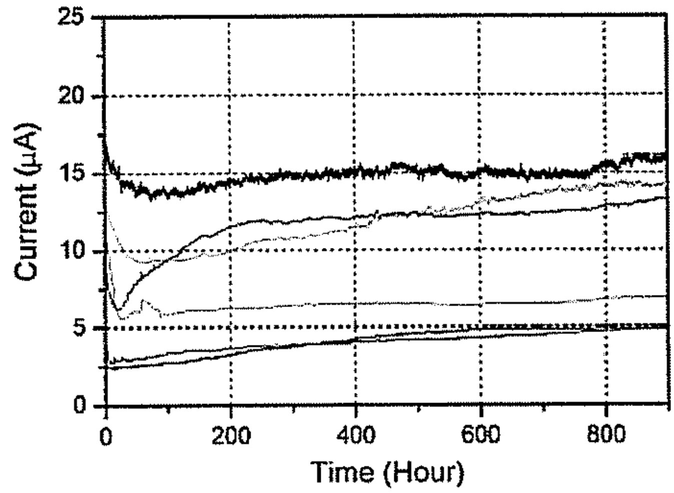

Figure 10

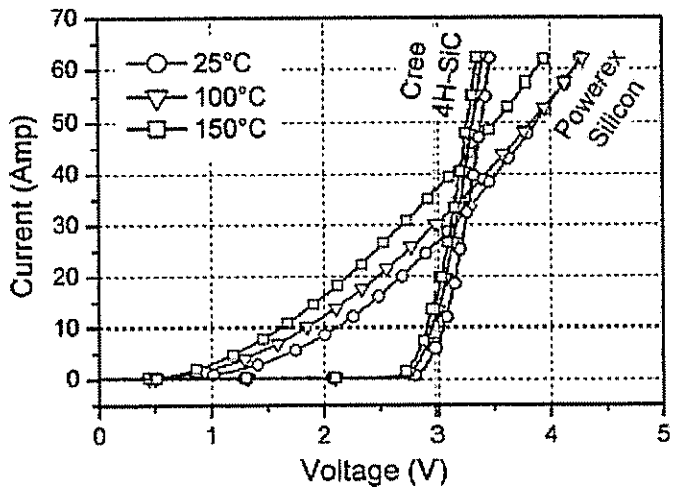

Figure 11

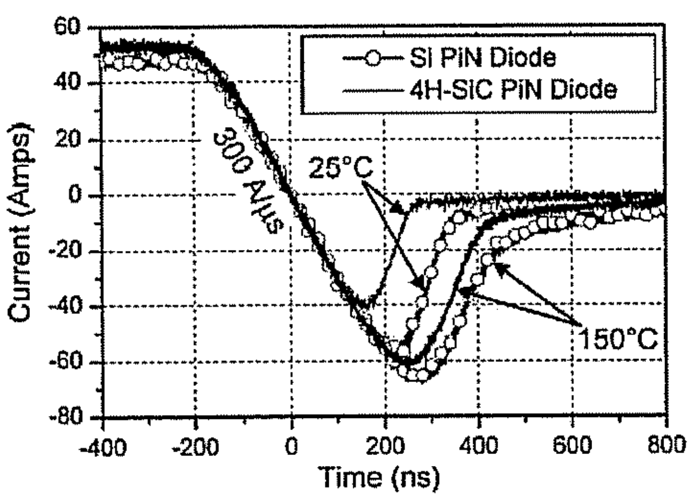

Figure 12

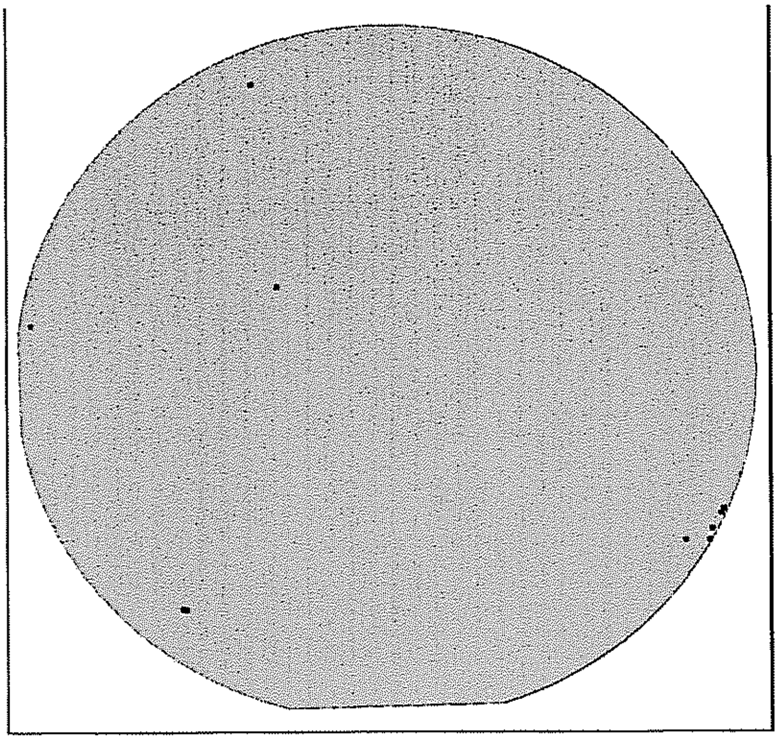

Figure 13

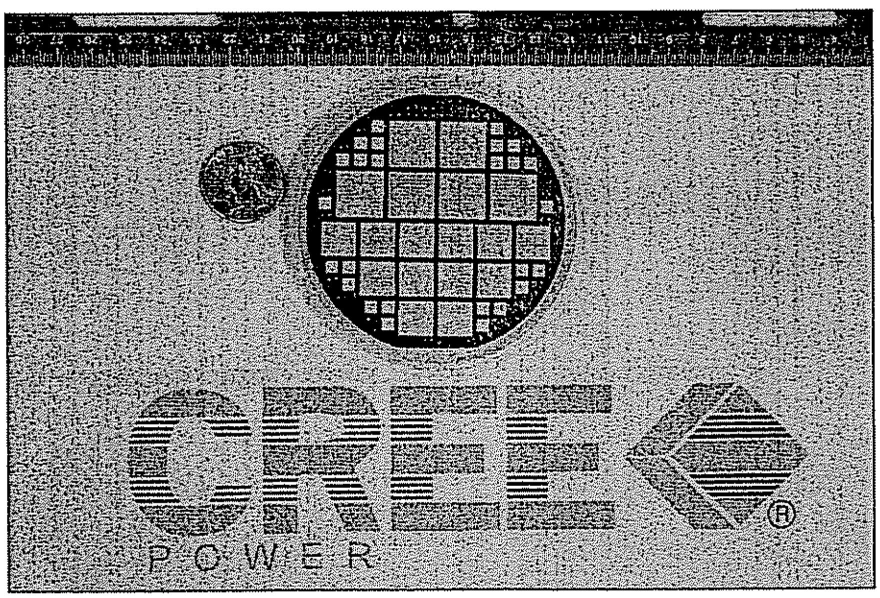

Figure 14

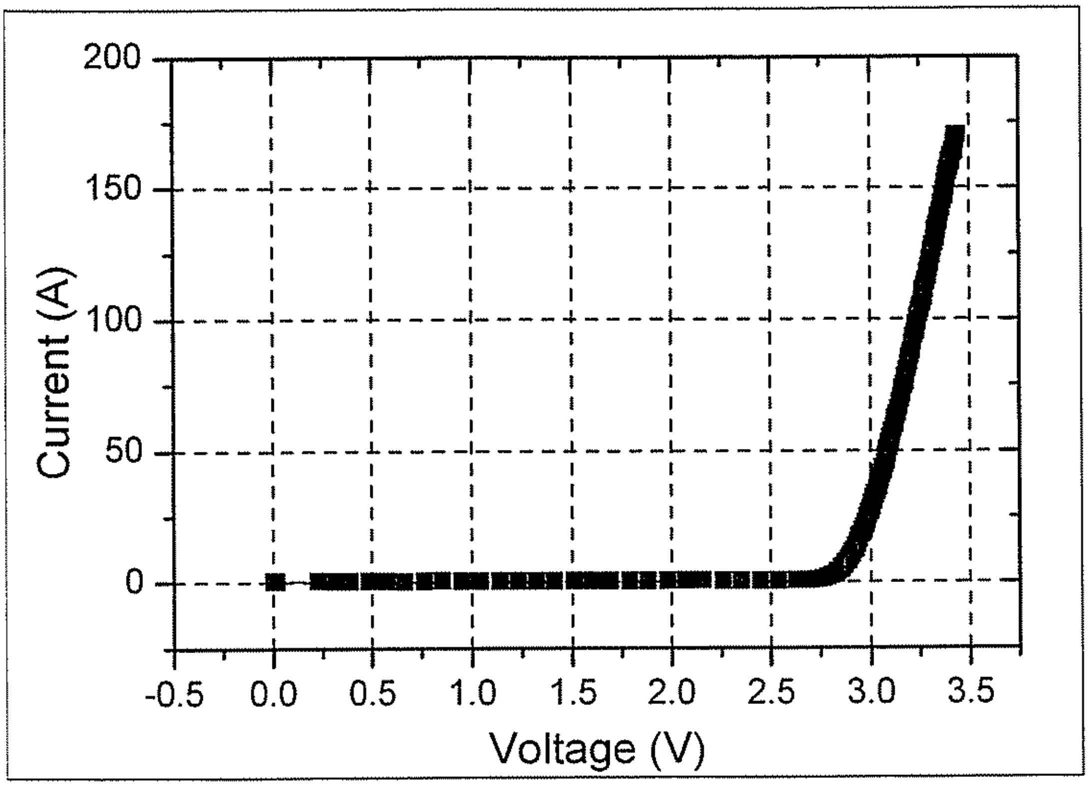

Figure 15

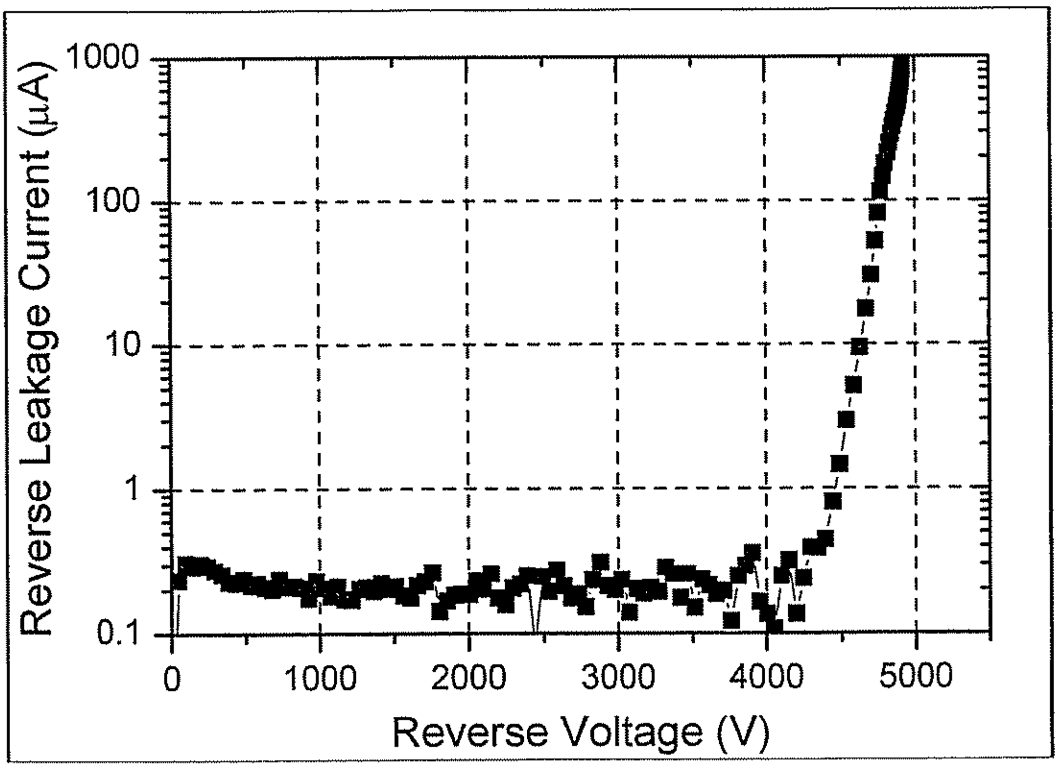

Figure 16

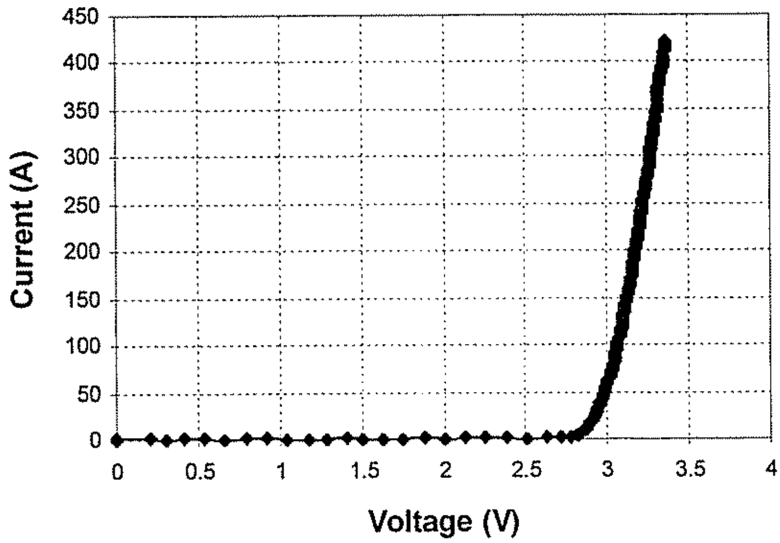

Figure 17

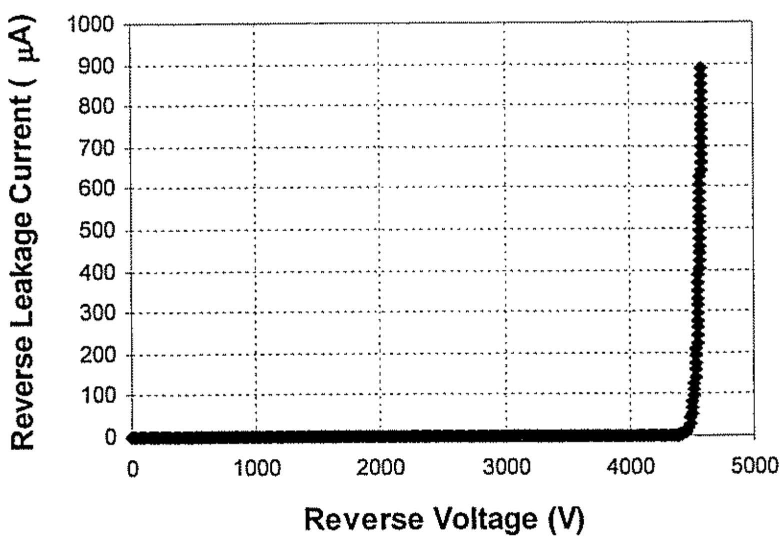

Figure 18

REPORT OF INVENTION

Pursuant to FAR 52.227-12(c)(1), this written report is being submitted to the Contracting Officer as an attachment to form DD-882 (or equivalent patent report form). As required, this report: (1) identifies the contract under which the invention was made; (2) identifies the inventor(s); (3) contains a description of the invention sufficiently complete in technical detail to convey a clear understanding of the nature, purpose, operation, and physical, chemical, biological, or electrical characteristics of the invention; (4) identifies any publication, on sale, or public use of the invention; and (5) identifies any anticipated publication, on sale, or public use of the invention.

Cree Reference No.	P0396
Title of Invention	Excess Silane Abatement Device
Inventor(s)	Michael O'Loughlin
Contracting Agency	Office of Naval Research (DARPA)
Contract No.	N00014-02-C-0302
Description of Invention	To reduce silane concentration in SiC epi reactor exhaust systems, a surface is provided within the ehaust path which removes silane from the gas flow. The surface may be a vane or wedge shape fixed within the center of the exhaust path.
Disclosures Outside of the Company*	None
Anticipated Disclosures Outside of the Company*	None

**Examples – publications, offers for sale, sales, discussions with suppliers or customers*

REPORT OF INVENTION

Pursuant to FAR 52.227-12(c)(1), this written report is being submitted to the Contracting Officer as an attachment to form DD-882 (or equivalent patent report form). As required, this report: (1) identifies the contract under which the invention was made; (2) identifies the inventor(s); (3) contains a description of the invention sufficiently complete in technical detail to convey a clear understanding of the nature, purpose, operation, and physical, chemical, biological, or electrical characteristics of the invention; (4) identifies any publication, on sale, or public use of the invention; and (5) identifies any anticipated publication, on sale, or public use of the invention.

Cree Reference No.	P0384
Title of Invention	Bulk Silicon Carbide Single Crystal Growth without Polycrystalline Rim
Inventor(s)	Valeri Tsvetkov, Mark Brady
Contracting Agency	Office of Naval Research (DARPA)
Contract No.	N00014-02-C-0302
Description of Invention	Apparatus for bulk growth of SiC via sublimation includes a seed holder and seed cap surmounting a cylindrical growth chamber. The interior lining of the cylindrical growth chamber comprises a filler ring that defines a space into which the crystal grows. The filler ring is formed of high-density rigid/solid carbon that resists etching and silicon vapor prenetration, resulting in reduced formation of polycrystalline material in the growth chamber and in the growing crystal.
Disclosures Outside of the Company*	None
Anticipated Disclosures Outside of the Company*	None

**Examples – publications, offers for sale, sales, discussions with suppliers or customers*

REPORT OF INVENTION

Pursuant to FAR 52.227-12(c)(1), this written report is being submitted to the Contracting Officer as an attachment to form DD-882 (or equivalent patent report form). As required, this report: (1) identifies the contract under which the invention was made; (2) identifies the inventor(s); (3) contains a description of the invention sufficiently complete in technical detail to convey a clear understanding of the nature, purpose, operation, and physical, chemical, biological, or electrical characteristics of the invention; (4) identifies any publication, on sale, or public use of the invention; and (5) identifies any anticipated publication, on sale, or public use of the invention.

Cree Reference No.	P0383
Title of Invention	Reduction of Cracking Rate in Silicon Carbide Crystals
Inventor(s)	Valeri Tsvetkov, Mark Brady
Contracting Agency	Office of Naval Research (DARPA)
Contract No.	N00014-02-C-0302
Description of Invention	A SiC sublimation system includes a crucible comprising a graphite barrel defining a cylindrical growth chamber surmounted by a seed holder which holds a SiC seed crystal and a graphite lid. A filler ring is disposed within the barrel such that the inner diameter of the filler ring is very close to the outer diameter of the seed crystal. The filler ring eliminates space for polycrystalline material to form on the outer edge of the growin gseed crystal, reducing tension stress in the grown crystal after cool-down.
Disclosures Outside of the Company*	None
Anticipated Disclosures Outside of the Company*	None

**Examples – publications, offers for sale, sales, discussions with suppliers or customers*

CREE

ATTORNEY-CLIENT PRIVILEGED AND CONFIDENTIAL

Filing Recommendation		**For IP Committee Use**
IP Committee Review Date:		Disclosure Number: P0475
Committee Recommendation: ☐ File: Disclosure Complete ☐ File: Prepare Full Disclosure ☐ Do Not File	☐ Publish Without Filing ☐ Review Further ☐ Keep as Trade Secret	Date Opened: MCS 7/6/04
Comments:		

Invention Disclosure	To: Associate General Counsel for Intellectual Property

1. Invention Title: Process method for manufacturing high minority lifetime bulk-grown SiC materials.

2. Inventors:

	Inventor No. 1	Inventor No. 2	Inventor No. 3
Full name	Calvin Carter	Jason Jenny	Dave Malta
Home Address		(b) (6) [redacted]	(b) (6) [redacted]
Work Phone	(b) (6) [redacted]	(b) (6) [redacted]	(b) (6) [redacted]
Citizenship	USA	USA	USA
Department	Crystal Growth	Crystal Growth	Crystal Growth
Manager	Himself	Don Hobgood	Don Hobgood
Wrote Disclosure	☐ Yes ☒ No	☒ Yes ☐ No	☐ Yes ☒ No
	Inventor No. 4		
Full name Home Address	Hudson McD. Hobgood		
Work Phone	(b) (6) [redacted]		
Citizenship	USA		
Department	Crystal Growth		
Manager	Rob Glass		
Wrote Disclosure	☐ Yes ☒ No	☐ Yes ☐ No	☐ Yes ☐ No

Attach additional sheets if necessary

3. Date invention conceived: 4/1/04 Date invention reduced to practice: 4/10/04

4. Invention developed under government contract? Yes ☒ No ☐ Internal Contract No.: 1118

IMPORTANT: If you have any question as to whether the invention was developed (i.e. conceived or first reduced to practice) under a government contract, please contact the contract manager.

5. Identify any disclosures of the invention outside the company. For example, identify any publication, abstract, offer for sale or sale, discussions with suppliers or customers, etc., in which the invention was described. Give the date and place of any such disclosures. (attach additional sheets if necessary): no disclosures of the invention outside the company

(b) (6) [redacted]	Date	Witnessed, read and understood:	Date
	/6/04	(1)	
	6/04	(2)	
	6/04	(3)	
	6/04	(4)	

PFI Rev.8/2002

6. Identify any anticipated disclosures of the invention outside the company.: no anticipated disclosures of the invention outside the company

7. Identify any related inventions or disclosures by Cree personnel: no related inventions or disclosures by Cree personal

8. Identify products in which the invention may be used: power devices which require long minority carrier lifetimes for operation.

Remember to have each page of your invention disclosure signed and dated by a witness.
Please attach this cover form to your invention disclosure, along with any relevant documentation. Submit the disclosure to David Hall, Silicon Drive x5343.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) [redacted]	7/6/04	(1)	
(2)	7/6/04	(2)	
(3)	7/6/04	(3)	
(4)	7/6/04	(4)	

Description of Invention

Answer each of the following questions about your invention. Use additional space or attach additional sheets as necessary. Attach copies of notes, diagrams, lab notebooks, journal articles, etc. if available. Have a witness sign and date each sheet of the disclosure, including additional sheets.

1. Provide a brief description of the invention. What problem does it solve, and how does it solve the problem?

Currently, high minority carrier lifetime (MCL) SiC materials have only been produced via epitaxy. Certain devices such as PIN diodes require thick epitaxial layers whose thickness scales with the operating voltage. As the voltages move beyond 10 kV, these layers are problematic to grow and therefore quite expensive. A principal requirement for proper operation of these devices is that the MCL are sufficiently high (>3-5 μs) to allow for conductivity modulation. The purpose of this invention is to have a process which transforms more economically produced bulk-grown substrate materials into high MCL material. Typical lifetimes for bulk grown materials are below 10 ns (Fig. 1). This invention transforms bulk-grown HPSI material into a high MCL material with a lifetime in excess of 30 μs (Fig. 2).

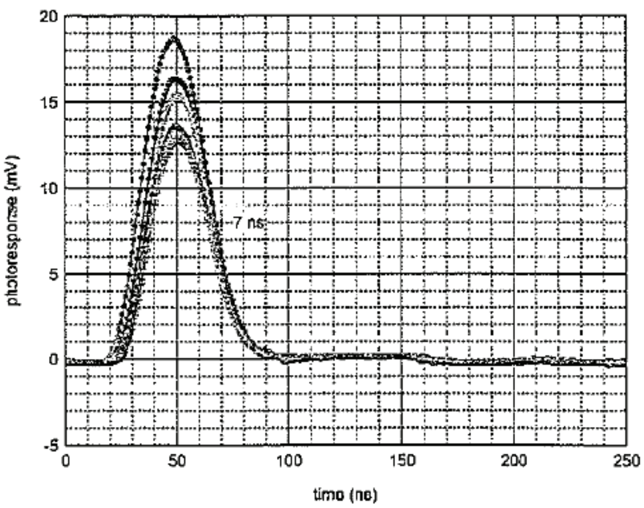

Figure 1 - Microwave PCD of a typical bulk-grown substrate

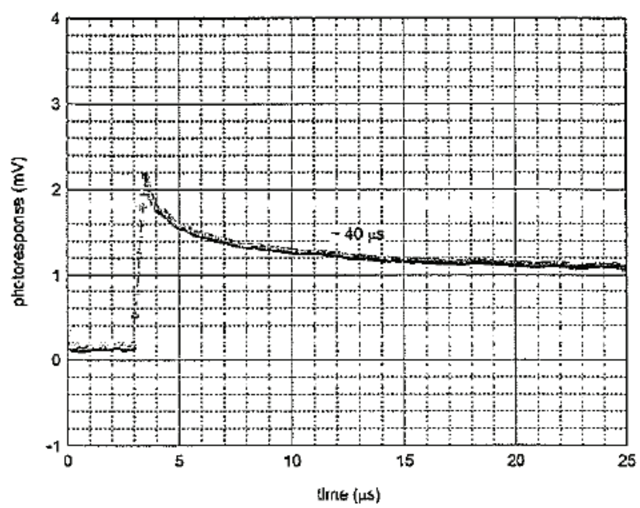

Figure 2 - Microwave PCD of a bulk-grown substrate with new process

2. How does the invention differ from present technology? What are the novel or unusual features of the invention? What advantages does it possess?

This method is a very high temperature anneal after crystal growth. It is novel in that it generates high MCL material from an anneal at temperatures higher than its growth temperature.

3. Describe specific embodiments or examples of the invention, if any. Does the invention have any alternative embodiments? Enclose sketches, drawings, photographs and other materials that help illustrate the description.

[redacted]	Date	Witnessed, read and understood:	Date
	7/6/04	(1)	
	7/6/04	(2)	
	7/6/04	(3)	
	7/2/04	(4)	

To apply the method of this invention, a SiC substrate (or crystal) is heated to a temperature in excess of its growth temperature (e.g. 2600°C) and cooled in a sufficiently slow manner to prevent the significant introduction of deep level trapping defects.

This invention may be applied to epitaxially-grown material to enhance MCLs in that material.

4. What are possible applications for the invention? In addition to immediate applications, are there other uses that might be feasible in the future?

   This can be used for any device which requires high MCL materials.

5. List any documents or publications which relate to important aspects of this invention.

   P0137, P0232/P0232US2

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
[redacted]	7/6/04	(1)	
	7/6/04	(2)	
	7/6/04	(3)	
	7/6/04	(4)	

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ATTORNEY-CLIENT PRIVILEGED AND CONFIDENTIAL

Filing Recommendation	For IP Committee Use
IP Committee Review Date:	Disclosure Number: P0414
Committee Recommendation: ☐ File: Disclosure Complete ☐ Publish Without Filing ☐ File: Prepare Full Disclosure ☐ Review Further ☐ Do Not File ☐ Keep as Trade Secret	Date Opened: mcs 3/16/04
Comments:	

Invention Disclosure

To: Associate General Counsel for Intellectual Property

1. Invention Title: Lithographic method to reduce stacking fault nucleation sites and reduce Vf drift in Bipolar devices.

2. Inventors.

	Inventor No. 1	Inventor No. 2	Inventor No. 3
Full name	Joseph John Sumakeris	Mrinal Das	
Home Address	[redacted]		
Work Phone	[redacted]		
Citizenship	USA		
Department	SiC Epi		
Manager	Robert Glass		
Wrote Disclosure	☒ Yes ☐ No	☐ Yes ☐ No	☐ Yes ☐ No

Attach additional sheets if necessary

3. Date invention conceived: Tech. Developed by ABB and Linkoping, University 13 1C95
Date invention reduced to practice: December 9, 2003 (at Cree)

4. Invention developed under government contract? Yes ☒ No ☐ Internal Contract No.: N00014-02-C-0302

IMPORTANT: If you have any question as to whether the invention was developed (i.e. conceived or first reduced to practice) under a government contract, please contact the contract manager.

5. Identify any disclosures of the invention outside the company. For example, identify any publication, abstract, offer for sale or sale, discussions with suppliers or customers, etc., in which the invention was described. Give the date and place of any such disclosures. (attach additional sheets if necessary): Technology transferred to Cree during technology transfer with ABB.

6. Identify any anticipated disclosures of the Invention outside the company.: Regular reporting to Darpa Agency

7. Identify any related inventions or disclosures by Cree personnel: Previous disclosure on Vf Drift Control via Stacking Fault Pinning from Oct. 2001. Previous disclosure on etching wafers tominimize stacking fault nucleation sites, April, 2003

8. Identify products in which the invention may be used: Bipoar devices in SiC or other materials subject to recombination enhanced dislocation glide. Devices sensitive to the presence of basal plane dislocations

Remember to have each page of your invention disclosure signed and dated by a witness.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1)	
(2)		(2)	
(3)		(3)	

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CREE

ATTORNEY-CLIENT PRIVILEGED AND CONFIDENTIAL

Please attach this cover form to your invention disclosure, along with any relevant documentation. Submit the disclosure to David Hall, Silicon Drive x5343.

Description of Invention

Answer each of the following questions about your invention. Use additional space or attach additional sheets as necessary. Attach copies of notes, diagrams, lab notebooks, journal articles, etc. if available. Have a witness sign and date each sheet of the disclosure, including additional sheets.

1. Provide a brief description of the invention. What problem does it solve, and how does it solve the problem?

Commercial quality SiC wafers and epilayers contain a number of crystallographic defects. Most notable of the defects present in substrates are dislocations, including screw (closed and open core) and edge dislocations. These dislocations can be further grouped by their alignment within the crystal. Those dislocations that propagate along the c-axis are called threading dislocations, while dislocations that lie within the c-plane are termed basal plane dislocations. In general, in SiC, it is energetically favorable that basal plane dislocations preferentially decompose into partial dislocations via the mechanism described below:

$$1/3\langle 11\bar{2}0\rangle \rightarrow 1/3\langle 10\bar{1}0\rangle + 1/3\langle 01\bar{1}0\rangle \qquad \text{Equation 1}$$

In general, the above decomposition reaction describes the decomposition of a basal plane dislocation into two Shockley partial dislocations. The line defects generated during the above decomposition will bound a planar stacking fault defect. This stacking fault will be electrically active in bipolar devices and during forward operation, the electron-hole plasma will be reduced in the vicinity of the stacking fault. The reduced plasma density will increase the forward voltage of the device. A further complication is that through dislocation enhanced dislocation glide, the stacking fault may continue to expand during forward operation of the device. As a result, during continued operation, the forward voltage of the device can increase substantially from the initial value as shown in Figure 1 In Figure 1, we plot forward voltage as it changes with time. As the device warms to operating temperature, it is expected that the V_f will decrease slightly, however, note that two diodes experience substantial V_f increase. This behavior is a substantial barrier to device exploitation because it results in devices with functional properties that can change unpredictably during operation.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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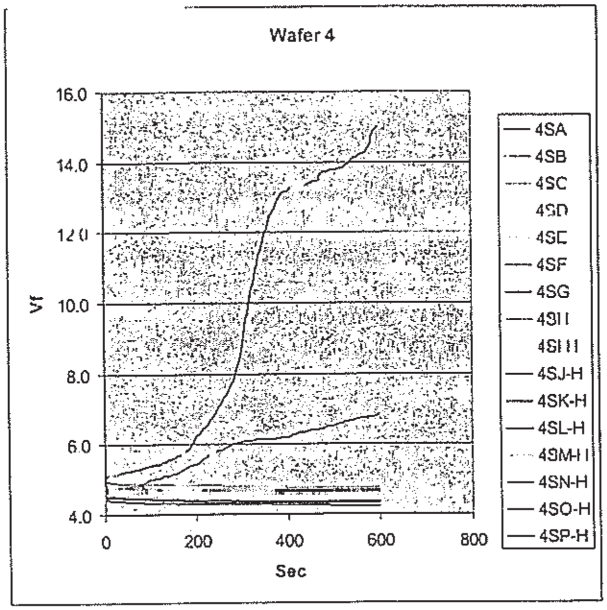

Figure 1. Plot of forward voltage vs operation time for 16 diodes. 14 are stable, 2 drift unacceptably.

Commercially available 4H-SiC substrates have approximately 1E4 to 1E5 dislocations per cm^2. This includes threading screw and edge dislocations and basal plane dislocations. Figure 2 is a micrograph of KOH etched epilayer surface revealing various common types of dislocation pits which are labeled appropriately. All types of dislocations can potentially impact device performance, but the basal plane dislocation is particularly implicated as being the prevalent nucleation site of the stacking faults that cause V_f drift.

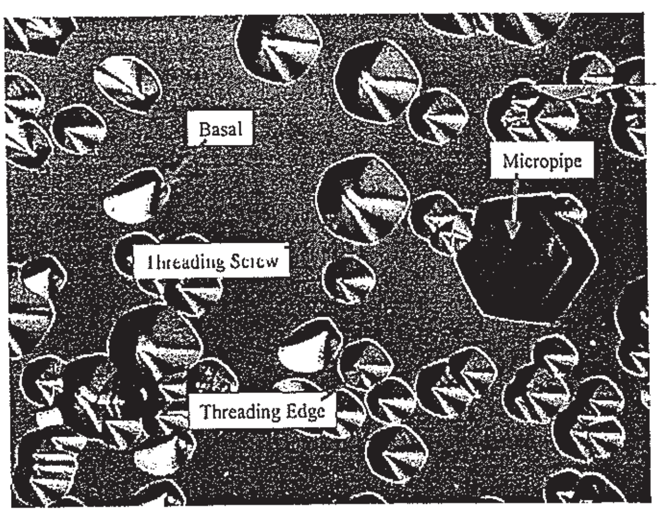

Figure 2. Etch pits on 4H-SiC epilayer.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1)	
(2)		(2)	
(3)		(3)	

Previous disclosures listed in section 7 concerned techniques to reduce the density of basal plane dislocation density in epilayers. The current invention is very similar in scope to the KOH etch step central to the Method to reduce stacking fault nucleation sites and reduce Vf drift in Bipolar devices disclosure except a dry etch is employed and the etching is not self aligned, but rather is defied by an engineered mask.

By etching a series of steps into the off-axis growth face, it is possible to encourage a large portion of the basal plane dislocations present in the substrate or underlying epi to convert to threading edge dislocations which are not as problematic for achieving V_f stability. We have tested two geometry's of etch as shown in Figure 3, but so far have full results only for one geometry, the "hex etch" pattern.

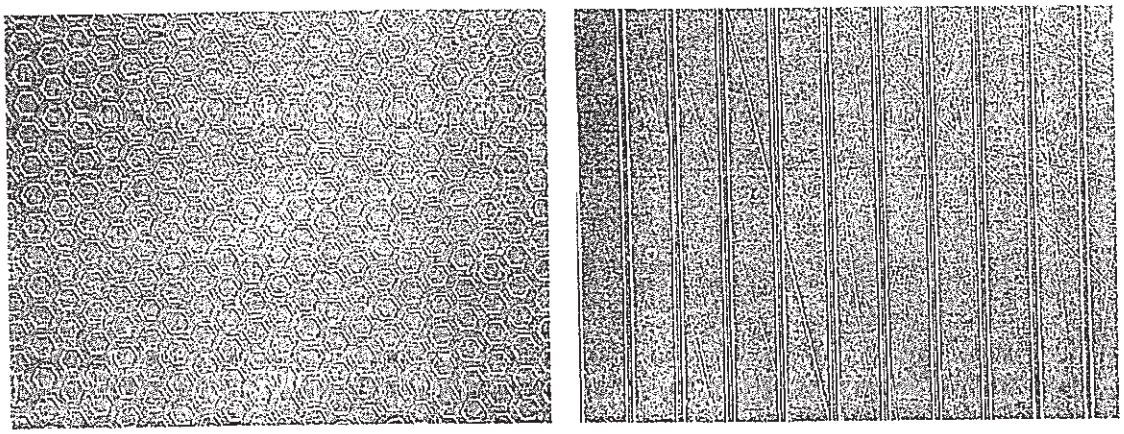

Figure 3. Hex etch (left) and line etch (right) template patterns for BPD turning
The epilayer surfaces after growth are depicted in Figure 4 for the hex etch and for the line etch templates, respectively.

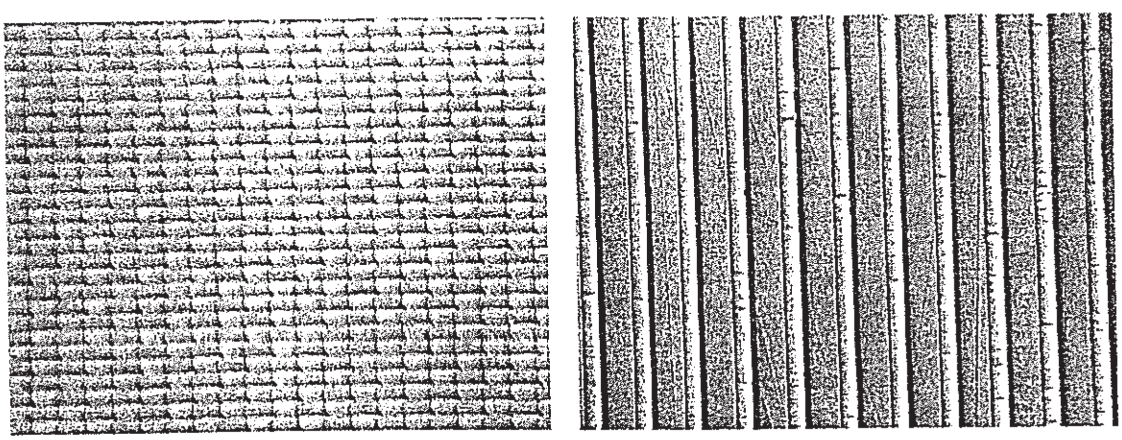

Figure 4. Epi surface after growth on hex etch (left) and line etch (right) templated surfaces

We have KOH etched epi samples grown using our original low BPD process and the hex-etch process (Figure 5) and find that both approaches are effective in their ability to convert BPDs to threading dislocations.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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(3)		(3)	

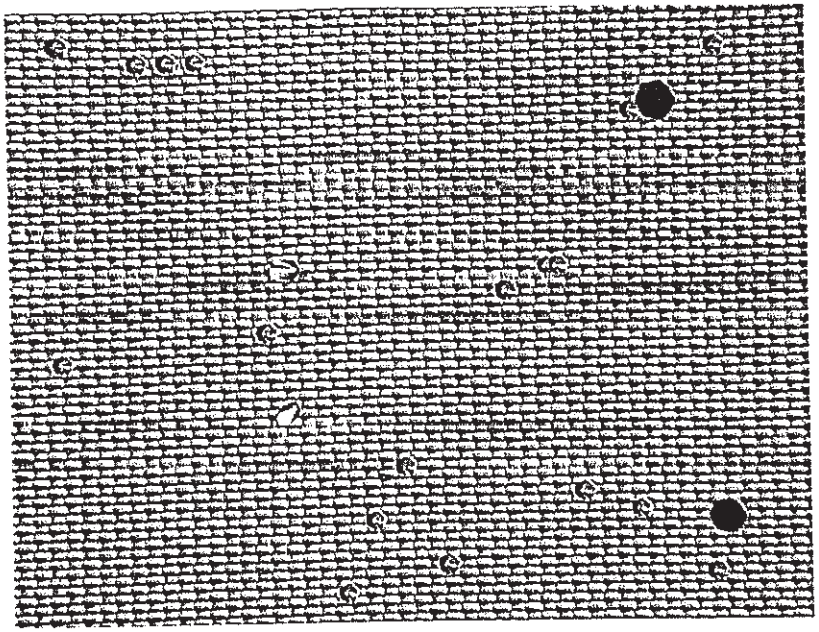


Figure 5. KOH etched epilayer grown on a hex-etch templated surface revealing characteristic dislocation etch pits.

We have also fabricated devices using the hex-etch template and V_f drift results are presented in Figure 6. The data in Figure 6 all comes from a single wafer where half of the wafer was prepared with the hex-etch pattern prior to epilayer growth while the remaining half of the wafer had no special treatment. It is evident in the plot that only 2 of the 8 standard prep diodes had a stable (or showed the characteristic slightly decreasing) V_f during the course of the test. Meanwhile, 5 of the 8 diodes grown on the hex-etch prepared surface showed a stable V_f.

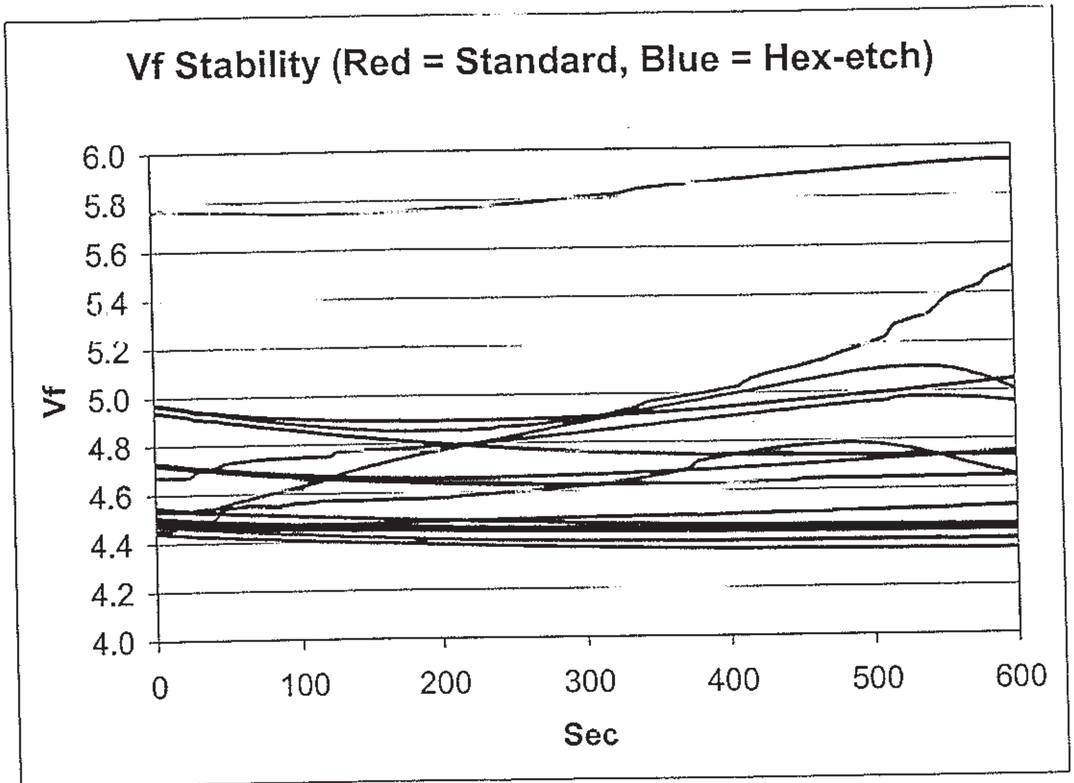
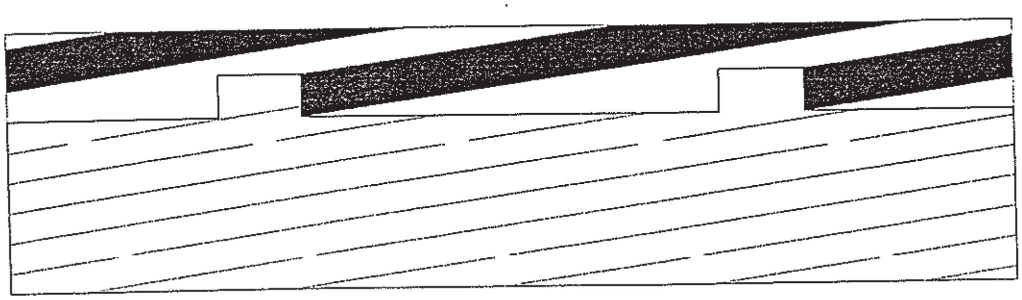


Figure 6. V_f stability of standard prep and hex-etch prepared 10 kV class PiN diodes

This is a very encouraging result. Although in this first test of the hex-etch for producing PiN diodes, we did not get as good a result in terms of stabilizing V_f as we do with the KOH etch, we expect that we will achieve better results by improving the etch geometry and application For example, the wall width in the hex-etch pattern is greater than preferable as will be discussed below.

The intent of the invention is to initially nucleate the epilayer on the side-wall of the etch pattern as shown in Figure 7. In this way a very facile environment for BPD turning is created. It should be noted that material starting to grow on the top of the wall or in the plateau between walls would not benefit fully from this improved growth geometry. Consequently, the wall top area, step height and spacing should be optimized. In addition, we are evaluating multiple applications of the hex and line-etch processes. Note that in Figure 7, only portions of the epilayer are advantaged by a single iteration of the application. Repeat iterations and optimizing of geometry is expected to yield improved benefits.



Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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(2)		(2)	
(3)		(3)	

Figure 7. Schematic of line-etch pattern and resultant epi. Material in the red region benefits from enhanced BPD turning as growth proceeds on sides of walls defined in substrate.

2. How does the invention differ from present technology? What are the novel or unusual features of the invention? What advantages does it possess?

The best current approach to limiting BPDs in device epilayers employs a KOH etch. A major disadvantage of the KOH etch is that in addition to the advantageous decoration of BPDs that that process seeks, other defects are also decorated by KOH etch. For example, KOH etching generates pits associated with micropipes and threading dislocations that can be very deep. It is very likely that epilayers grown over such surfaces would have higher than normal epilayer defect densities. Further, the current best low BPD process employs repeat KOH etch and polish steps. This makes for very complicated, time consuming and expensive process route.

The advantage of the hex and line-etch processes is that they are accomplished with relatively typical fabrication processes employing lithography and dry etching. Further, excessively deep pits are not generated in the invention, so only minimal, perhaps no polish post treatment is necessary for high voltage devices.

3. Describe specific embodiments or examples of the invention, if any. Does the invention have any alternative embodiments? Enclose sketches, drawings, photographs and other materials that help illustrate the description

The invention can be accomplished with alternative etch processes, but RIE is preferable. Many different etch patterns can be considered such as the hexes, line, herringbone, etc.

4. What are possible applications for the invention? In addition to immediate applications, are there other uses that might be feasible in the future?

The approach can be of value for the production of any semiconductor device which may experience V_f drift or performance degradation similar to V_f drift such as recombination enhanced dislocation glide.

5. List any documents or publications which relate to important aspects of this invention.

Technology transfer materials from ABB.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1)	
(2)		(2)	
(3)		(3)	

CREE

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Filing Recommendation	For IP Committee Use
IP Committee Review Date:	Disclosure Number: P0414
Committee Recommendation: ☐ File: Disclosure Complete ☐ Publish Without Filing ☐ File: Prepare Full Disclosure ☐ Review Further ☐ Do Not File ☐ Keep as Trade Secret	Date Opened: MCS 3/16/04
Comments	

Invention Disclosure

To: Associate General Counsel for Intellectual Property

1. Invention Title: Lithographic method to reduce stacking fault nucleation sites and reduce Vf drift in Bipolar devices.
2. Inventors:

	Inventor No. 1	Inventor No. 2	Inventor No. 3
Full name	Joseph John Sumakeris	Mrinal Das	
Home Address	[redacted]		
Work Phone	[redacted]		
Citizenship	USA		
Department	SiC Epi		
Manager	Robert Glass		
Wrote Disclosure	☒ Yes ☐ No	☐ Yes ☐ No	☐ Yes ☐ No

Attach additional sheets if necessary

3. Date invention conceived: Tech. Developed by ABB and Linkoping, University
   Date invention reduced to practice: December 9, 2003 (at Cree) 93 - 1095

4. Invention developed under government contract? Yes ☒ No ☐ Internal Contract No.: N00014-02-C-0302
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7. Identify any related inventions or disclosures by Cree personnel: Previous disclosure on Vf Drift Control via Stacking Fault Pinning from Oct. 2001. Previous disclosure on etching wafers tominimize stacking fault nucleation sites, April, 2003

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Remember to have each page of your invention disclosure signed and dated by a witness.

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PF1 Rev.8/2002

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In general, the above decomposition reaction describes the decomposition of a basal plane dislocation into two Shockley partial dislocations. The line defects generated during the above decomposition will bound a planar stacking fault defect. This stacking fault will be electrically active in bipolar devices and during forward operation, the electron-hole plasma will be reduced in the vicinity of the stacking fault. The reduced plasma density will increase the forward voltage of the device. A further complication is that through dislocation enhanced dislocation glide, the stacking fault may continue to expand during forward operation of the device. As a result, during continued operation, the forward voltage of the device can increase substantially from the initial value as shown in Figure 1. In Figure 1, we plot forward voltage as it changes with time. As the device warms to operating temperature, it is expected that the V_f will decrease slightly, however, note that two diodes experience substantial V_f increase. This behavior is a substantial barrier to device exploitation because it results in devices with functional properties that can change unpredictably during operation.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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(2)		(2)	
(3)		(3)	

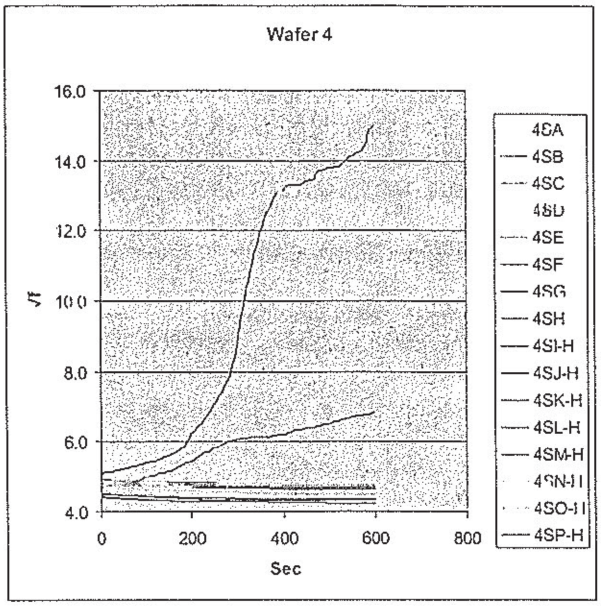

Figure 1. Plot of forward voltage vs operation time for 16 diodes. 14 are stable, 2 drift unacceptably.

Commercially available 4H-SiC substrates have approximately 1E4 to 1E5 dislocations per cm^2. This includes threading screw and edge dislocations and basal plane dislocations. Figure 2 is a micrograph of KOH etched epilayer surface revealing various common types of dislocation pits which are labeled appropriately. All types of dislocations can potentially impact device performance, but the basal plane dislocation is particularly implicated as being the prevalent nucleation site of the stacking faults that cause V_f drift.

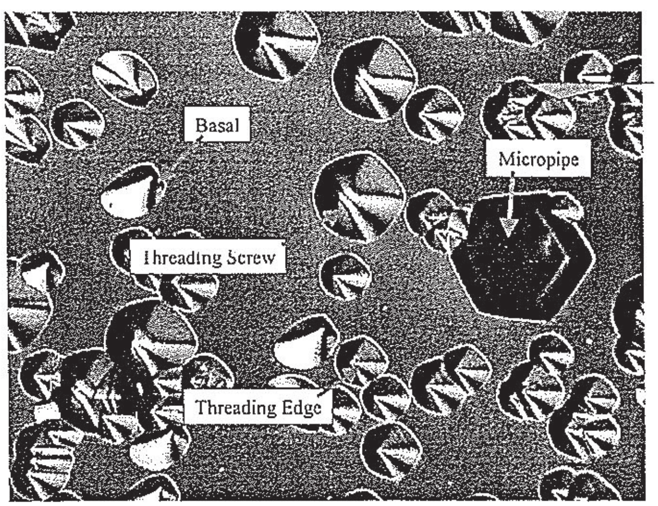

Figure 2. Etch pits on 4H-SiC epilayer.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1)	
(2)		(2)	
(3)		(3)	

Previous disclosures listed in section 7 concerned techniques to reduce the density of basal plane dislocation density in epilayers. The current invention is very similar in scope to the KOH etch step central to the Method to reduce stacking fault nucleation sites and reduce Vf drift in Bipolar devices disclosure except a dry etch is employed and the etching is not self aligned, but rather is defied by an engineered mask.

By etching a series of steps into the off-axis growth face, it is possible to encourage a large portion of the basal plane dislocations present in the substrate or underlying epi to convert to threading edge dislocations which are not as problematic for achieving V_f stability. We have tested two geometry's of etch as shown in Figure 3, but so far have full results only for one geometry, the "hex etch" pattern.

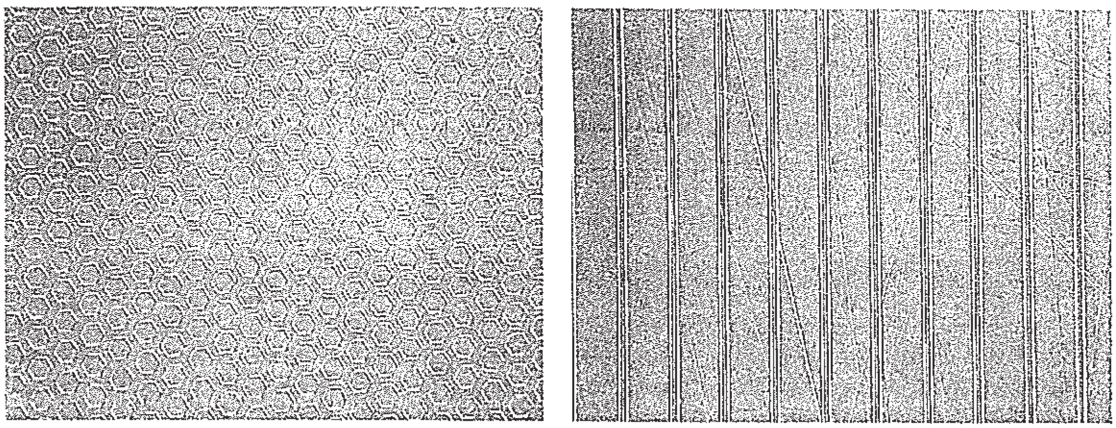

Figure 3. Hex etch (left) and line etch (right) template patterns for BPD turning

The epilayer surfaces after growth are depicted in Figure 4 for the hex etch and for the line etch templates, respectively.

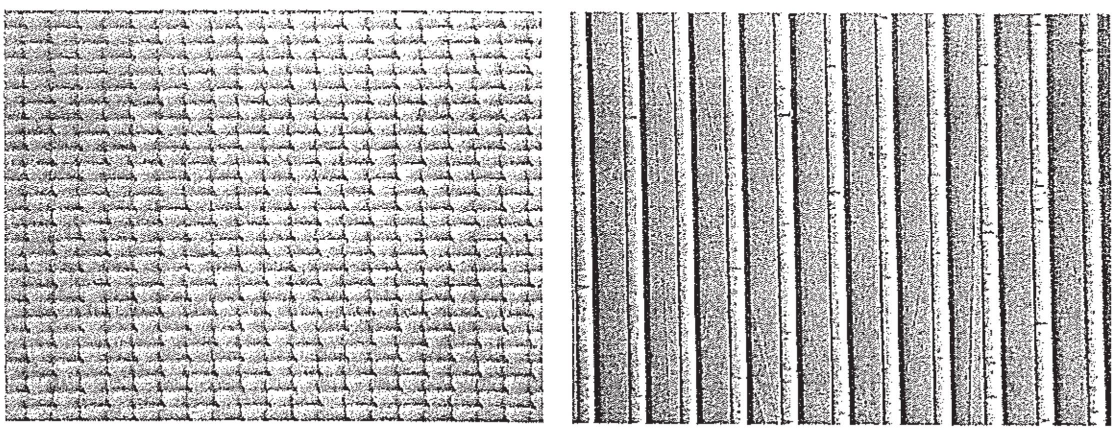

Figure 4. Epi surface after growth on hex etch (left) and line etch (right) templated surfaces

We have KOH etched epi samples grown using our original low BPD process and the hex-etch process (Figure 5) and find that both approaches are effective in their ability to convert BPDs to threading dislocations.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1)	
(2)		(2)	
(3)		(3)	

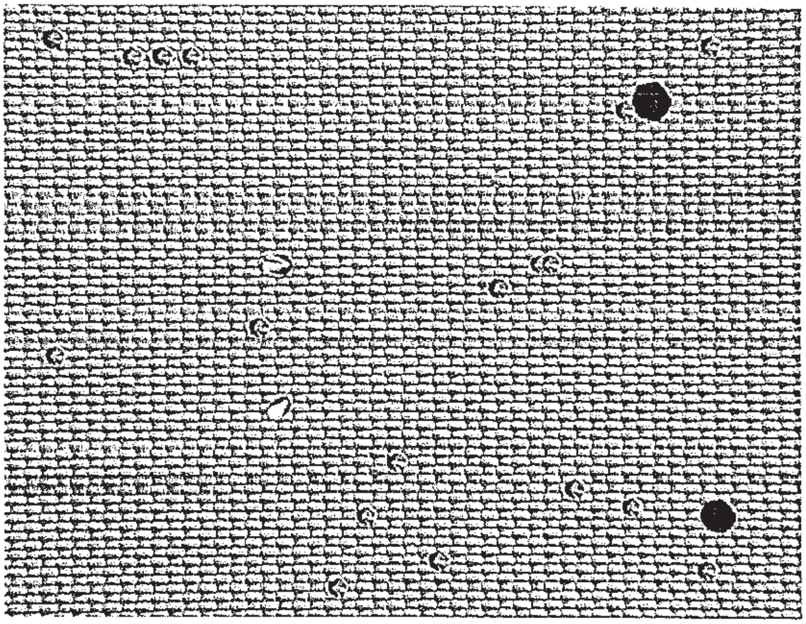

Figure 5. KOH etched epilayer grown on a hex-etch templated surface revealing characteristic dislocation etch pits.

We have also fabricated devices using the hex-etch template and V_f drift results are presented in Figure 6. The data in Figure 6 all comes from a single wafer where half of the wafer was prepared with the hex-etch pattern prior to epilayer growth while the remaining half of the wafer had no special treatment. It is evident in the plot that only 2 of the 8 standard prep diodes had a stable (or showed the characteristic slightly decreasing) V_f during the course of the test. Meanwhile, 5 of the 8 diodes grown on the hex-etch prepared surface showed a stable V_f.

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(2)		(2)	
(3)		(3)	

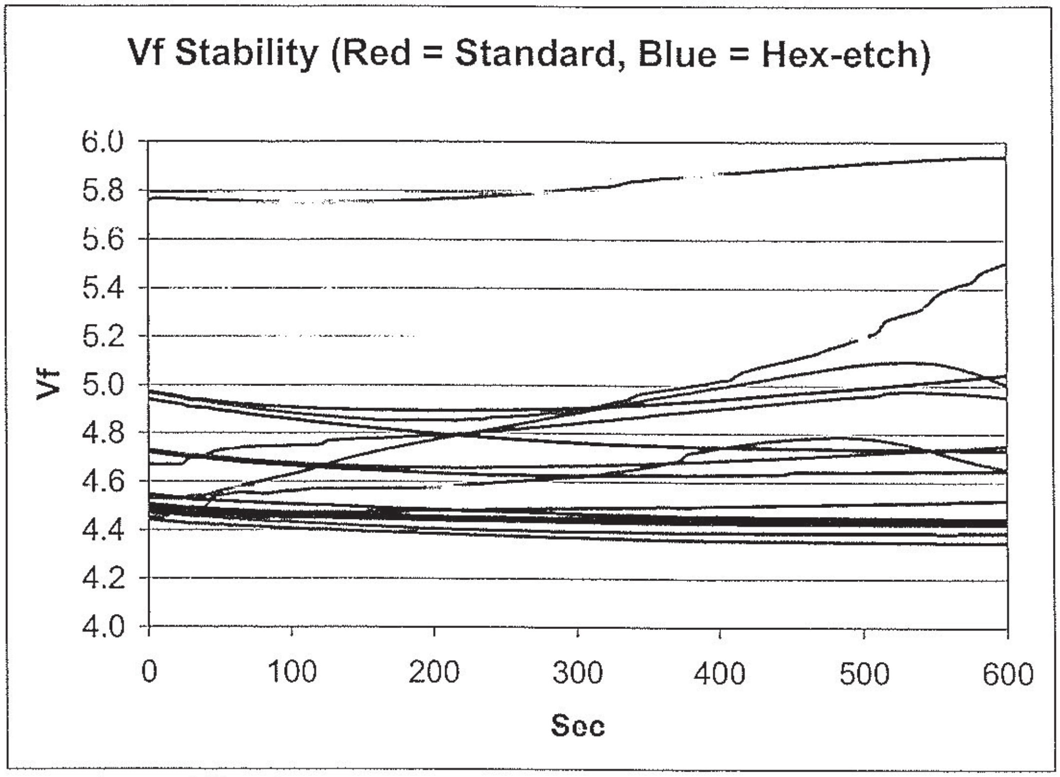
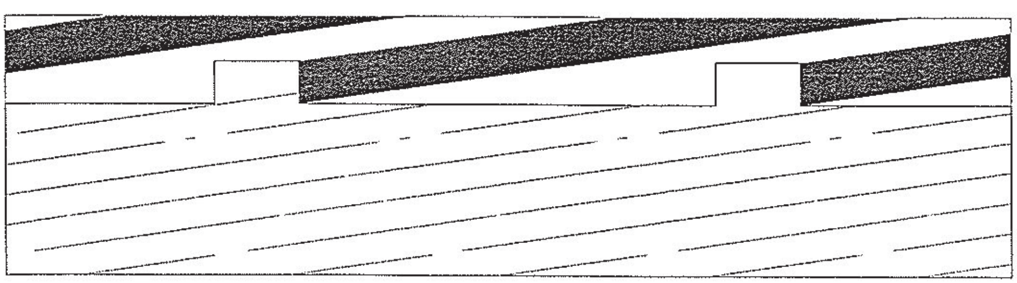


Figure 6. V_f stability of standard prep and hex-etch prepared 10 kV class PiN diodes

This is a very encouraging result. Although in this first test of the hex-etch for producing PiN diodes, we did not get as good a result in terms of stabilizing V_f as we do with the KOH etch, we expect that we will achieve better results by improving the etch geometry and application. For example, the wall width in the hex-etch pattern is greater than preferable as will be discussed below.

The intent of the invention is to initially nucleate the epilayer on the side-wall of the etch pattern as shown in Figure 7. In this way a very facile environment for BPD turning is created. It should be noted that material starting to grow on the top of the wall or in the plateau between walls would not benefit fully from this improved growth geometry. Consequently, the wall top area, step height and spacing should be optimized. In addition, we are evaluating multiple applications of the hex and line-etch processes. Note that in Figure 7, only portions of the epilayer are advantaged by a single iteration of the application Repeat iterations and optimizing of geometry is expected to yield improved benefits.



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(1)		(1)	
(2)		(2)	
(3)		(3)	

Figure 7. Schematic of line etch pattern and resultant epi. Material in the red region benefits from enhanced BPD turning as growth proceeds on sides of walls defined in substrate.

2. How does the invention differ from present technology? What are the novel or unusual features of the invention? What advantages does it possess?

   The best current approach to limiting BPDs in device epilayers employs a KOH etch. A major disadvantage of the KOH etch is that in addition to the advantageous decoration of BPDs that that process seeks, other defects are also decorated by KOH etch. For example, KOH etching generates pits associated with micropipes and threading dislocations that can be very deep. It is very likely that epilayers grown over such surfaces would have higher than normal epilayer defect densities. Further, the current best low BPD process employs repeat KOH etch and polish steps. This makes for very complicated, time consuming and expensive process route.

   The advantage of the hex and line-etch processes is that they are accomplished with relatively typical fabrication processes employing lithography and dry etching. Further, excessively deep pits are not generated in the invention, so only minimal, perhaps no polish post treatment is necessary for high voltage devices.

3. Describe specific embodiments or examples of the invention, if any. Does the invention have any alternative embodiments? Enclose sketches, drawings, photographs and other materials that help illustrate the description.

   The invention can be accomplished with alternative etch processes, but RIE is preferable. Many different etch patterns can be considered such as the hexes, line, herringbone, etc.

4. What are possible applications for the invention? In addition to immediate applications, are there other uses that might be feasible in the future?

   The approach can be of value for the production of any semiconductor device which may experience V_f drift or performance degradation similar to V_f drift such as recombination enhanced dislocation glide.

5. List any documents or publications which relate to important aspects of this invention.

   Technology transfer materials from ABB

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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(2)		(2)	
(3)		(3)	

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Filing Recommendation		**For IP Committee Use**
IP Committee Review Date:		Disclosure Number: P0383
Committee Recommendation: ☐ File: Disclosure Complete ☐ File: Prepare Full Disclosure ☐ Do Not File	☐ Publish Without Filing ☐ Review Further ☐ Keep as Trade Secret	Date Opened: mcs 10/17/03
Comments:		

Invention Disclosure

To: Associate General Counsel for Intellectual Property

1. Invention Title: Reduction of Cracking Rate in Silicon Carbide Crystals.

2. Inventors:

	Inventor No. 1	Inventor No. 2	Inventor No. 3
Full name	Valeri F. Tsvetkov	Mark Brady	
Home Address	[redacted]	[redacted]	
Work Phone	[redacted]	[redacted]	
Citizenship	USA	USA	
Department	110	300	
Manager	Don Hobgood	Don Hobgood	
Wrote Disclosure	☒ Yes	☒ Yes	☐ Yes ☐ No

Attach additional sheets if necessary

3 Date invention conceived: 09.04.03 Date invention reduced to practice: 09.06.03

4. Invention developed under government contract? Yes ☒ No ☐ Internal Contract No.: 1093

IMPORTANT: If you have any question as to whether the invention was developed (i.e. conceived or first reduced to practice) under a government contract, please contact the contract manager.

5. Identify any disclosures of the invention outside the company. For example, identify any publication, abstract, offer for sale or sale, discussions with suppliers or customers, etc., in which the invention was described. Give the date and place of any such disclosures (attach additional sheets if necessary): no disclosures of the invention outside the company

6. Identify any anticipated disclosures of the invention outside the company.: no anticipated disclosures of the invention outside the company

7. Identify any related inventions or disclosures by Cree personnel: no related inventions or disclosures by CREE personnel

8. Identify products in which the invention may be used: for the growth of low stress high quality large size SiC crystals

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) [redacted]	10.10.03	(1) [redacted]	10/13/03
(2)	10/10/03	(2)	
(3)		(3)	

PFI Rev.8/2002

Description of Invention

Answer each of the following questions about your invention. Use additional space or attach additional sheets as necessary. Attach copies of notes, diagrams, lab notebooks, journal articles, etc. if available. Have a witness sign and date each sheet of the disclosure, including additional sheets.

1. Provide a brief description of the invention. What problem does it solve, and how does it solve the problem?
2. [redacted]

[redacted]

[redacted]

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(1) [redacted]	10.10.03	(1) [redacted]	10/13/03
(2) [redacted]	10/10/03	(2) [redacted]	
(3)	/ /	(3) /	

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[redacted]

[redacted]

3. [redacted]

[redacted]

[redacted]

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) [redacted]	10.10.03	(1) [redacted]	10/23/03
(2)	10/10/03	(2)	
(3)		(3)	

PF1 Rev.8/2002

3. Describe specific embodiments or examples of the invention, if any. Does the invention have any alternative embodiments? Enclose sketches, drawings, photographs and other materials that help illustrate the description.

[redacted]

[redacted]

4. What are possible applications for the invention? In addition to immediate applications, are there other uses that might be feasible in the future?

[redacted]

5. List any documents or publications which relate to important aspects of this invention.

[redacted]

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) [redacted]	10.03	(1) [redacted]	10/15/03
(2)	10/10/03	(2)	
(3)		(3)	

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IP Committee Review Date:	Disclosure Number: D0250
Committee Recommendation: ☐ File: Disclosure Complete ☐ Publish Without Filing ☐ File: Prepare Full Disclosure ☐ Review Further ☐ Do Not File ☐ Keep as Trade Secret	Date Opened: MCS 3/20/03
Comments:	

Invention Disclosure

To: Associate General Counsel for Intellectual Property

1. Invention Title: Employ alternative crystal orientations to minimize V_f drift in bipolar devices

2. Inventors:

	Inventor No. 1	Inventor No. 2	Inventor No. 3
Full name	Joseph John Sumakeris	Michael James Paisley	Stephan Georg Mueller
Home Address	[redacted]	[redacted]	[redacted]
Work Phone	[redacted]	[redacted]	[redacted]
Citizenship	USA	USA	Germany
Department	SIC Epi	SIC Epi	Crystal Growth
Manager	Rob Glass	Rob Glass	Rob Glass
Wrote Disclosure	☒ Yes ☐ No	☐ Yes ☒ No	☐ Yes ☒ No

	Inventor No. 4	Inventor No. 5
Full name	Hudson McDonald Hobgood	Albert Augustus Burk, Jr
Home Address	[redacted]	[redacted]
Work Phone	[redacted]	[redacted]
Citizenship	USA	USA
Department	Crystal Growth	SiC Epi
Manager	Rob Glass	Rob Glass
Wrote Disclosure	☐ Yes ☒ No	☐ Yes ☒ No

Attach additional sheets if necessary

3. Date invention conceived: 11/27/2001 Date invention reduced to practice: Not Yet

4. Invention developed under government contract? Yes ☒ No ☐ Internal Contract No.: N00014 02 C 0302

IMPORTANT: If you have any question as to whether the invention was developed (i.e. conceived or first reduced to practice) under a government contract, please contact the contract manager.

Inventor's Full Signature	Date	Inventor's Full Signature	Date
(1) [redacted]	3/19/2003	(4) [redacted]	3/19/03
(2)	3/19/2003	(5)	3/19/03
(3)	3/19/2003	(6)	

3. Describe specific embodiments or examples of the invention, if any. Does the invention have any alternative embodiments? Enclose sketches, drawings, photographs and other materials that help illustrate the description.

Figure 1 depicts a series of stacking fault in a PiN diode fabricated using a relatively near basal plane oriented substrate. The actual angle and relative scales in the figure are exaggerated for clarity. Note that current passing from the top anode contact to the bottom substrate contact must either divert extensively around or cross the stacking faults. It should be noted that at an 8° off axis alignment as typically used for 4H SiC, the stacking fault can be expected to expand laterally about 8× the thickness of the drift region of the device.

For comparison, Figure 2 depicts a series of stacking faults in a PiN diode fabricated on a substrate that was fabricated such that the basal planes are perpendicular to the substrate surface, such as would be the case with a $(1\,1\bar{2}0)$ oriented substrate. Note that in Figure 2, the current may pass with minimal hindrance between the stacking faults. It is expected that the device in Figure 2 would experience reduced Vf drift due to stacking fault interference.

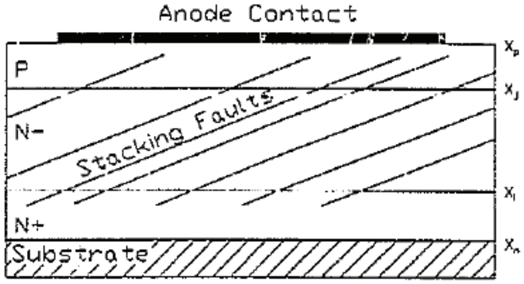

Figure 1. Stacking faults in diode made on conventional substrate.

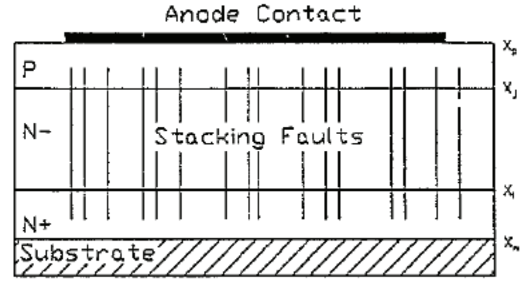

Figure 2. Stacking faults in diode made substrate with basal planes perpendicular to substrate surface.

4. What are possible applications for the invention? In addition to immediate applications, are there other uses that might be feasible in the future?

The invention is based on exploiting the crystallographic orientation of defects for optimal device fabrication and operation. Since many defects in crystals are crystallographically oriented, there can be many instances where judicious selection of substrate orientation will permit minimizing the deleterious effects of defects or optimizing directionally dependent materials properties such as carrier mobility.

5. List any documents or publications which relate to important aspects of this invention.

Proposal for Power DARPA contract.

Inventor's Full Signature	Date	Inventor's Full Signature	Date
(1) [redacted]	3/19/2003	(4) [redacted]	3/19/03
(2)	3/19/2003	(5)	3/19/03
(3)	3/18/2003	(6)	

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DECEMBER 19, 2006

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103343189A

CAROL PETROSKY
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875 NORTH RANDOLPH STREET
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SERIAL NUMBER: 10929911 FILING DATE: 08/30/2004
PATENT NUMBER: 7109521 ISSUE DATE: 09/19/2006
TITLE: SILICON CARBIDE SEMICONDUCTOR STRUCTURES INCLUDING MULTIPLE EPITAXIAL LAYERS HAVING SIDEWALLS

KIMBERLY WHITE, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

12-01-2006

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☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/929,911

B. Patent No.(s)

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State: VA Zip: 22203-1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

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4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/929,911

B. Patent No.(s)

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Silicon Carbide Semiconductor Structures Including Multiple Epitaxial Layers Having Sidewalls (as amended)

INVENTORS(S)
Sumakeris, Joesph
Hallin, Christer
Lendenmann, Heinz

SERIAL NO. P0477 10/929,911	FILING DATE 8/30/2004
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

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with

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(Seal)

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Cree, Inc
CONTRACTOR

(b) (6) [redacted]

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4600 Silicon Drive, Durham, NC 27703
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DECEMBER 15, 2006

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018638/0270
NUMBER OF PAGES: 2

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ASSIGNEE:
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OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10414787 FILING DATE: 04/16/2003
PATENT NUMBER: 7118781 ISSUE DATE: 10/10/2006
TITLE: METHODS FOR CONTROLLING FORMATION OF DEPOSITS IN A DEPOSITION SYSTEM AND DEPOSITION METHODS INCLUDING THE SAME

MARY BENTON, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Rev. 07/05)
)27 (exp. 6/30/2008)

12-01-2006

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City: ARLINGTON

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Additional name(s) & address(es) attached? ☐ Yes ☑ No

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Execution Date(s) 10/02/06

☐ Assignment ☐ Merger

☐ Security Agreement ☐ Change of Name

☐ Joint Research Agreement

☐ Government Interest Assignment

☑ Executive Order 9424, Confirmatory License

☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/414,787

B. Patent No.(s)

FINANCE

Additional numbers attached? ☐ Yes ☑ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY

Internal Address: OFFICE OF NAVAL RESEARCH

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Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

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OMB No. 0651-0027 (exp. 6/30/2008)

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Execution Date(s) 10/02/06

☐ Assignment ☐ Merger

☐ Security Agreement ☐ Change of Name

☐ Joint Research Agreement

☐ Government Interest Assignment

☑ Executive Order 9424, Confirmatory License

☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/414,787

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Methods and Apparatus for Controlling Formation of Deposits in a Deposition System and Deposition Systems and Methods Including the Same

INVENTORS(S)

Sumakeris, Joseph J.
Paisley, Michael P.
O'Loughlin, Michael J.

SERIAL NO. P0 297	10/414,787	FILING DATE 04/16/2003
CONTRACTOR Cree, Inc		CONTRACT NO. N00014-02-C-0302

The Invention Identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

with ______ included in Contract No. N00014-02-C-0302

Department of the Navy (ONR)
(specify government agency)

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Signed this 2nd day of October, 2006

ATTEST:

(Seal)

CREE, INC.
CORPORATE
SEAL
1987
NORTH CAROLINA

Cree, Inc
CONTRACTOR

[redacted]

CONTRACTOR'S OFFICIAL AND TITLE

4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECEMBER 15, 2006

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103343232A

CAROL PETROSKY
OFFICE OF NAVAL RESEARCH OFFICE OF ET AL
875 NORTH RANDOLPH STREET
ARLINGTON, VA 22203-1995

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018638/0290
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
CREE INCORPORATED DOC DATE: 10/02/2006

ASSIGNEE:
NAVY, SECRETARY OF THE UNITED
STATES OF AMERICA OFFICE OF
NAVAL RESEARCH
875 NORTH RANDOLPH STREET
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10698170 FILING DATE: 10/30/2003
PATENT NUMBER: ISSUE DATE:
TITLE: VERTICAL JFET LIMITED SILICON CARBIDE POWER METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS AND METHODS OF FABRICATING VERTICAL JFET LIMITED SILICON CARBIDE METAL- OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS

LAZENA MARTIN, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

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☐ Government Interest Assignment
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4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/698,170

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Vertical JFET Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors and Methods of Fabricating Vertical JFET Limited Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors

INVENTORS(S)

Sei-Hyung Ryu

SERIAL NO. D 0236, P 0279 10/698,170	FILING DATE 10/30/2003
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

with ________________________________ included in Contract No. N00014-02-C-0302

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ATTEST:

(Seal)

Cree, Inc
CONTRACTOR

[redacted] (b) (6)

CONTRACTOR'S OFFICIAL AND TITLE

4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

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DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECEMBER 15, 2006

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103343234A

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018638/0268
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
CREE INCORPORATED DOC DATE: 10/02/2006

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OFFICE OF NAVAL RESEARCH
875 NORTH RANDOLPH STREET
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 11147645 FILING DATE: 06/08/2005
PATENT NUMBER: ISSUE DATE:
TITLE: LOW BASAL PLANE DISLOCATION BULK GROWN SIC WAFERS

JOANN STEWART, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

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4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/147,645

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Low basal plane dislocation bulk grown SIC wafers

INVENTORS(S)

Adrian Powell, Mark Brady, and Valeri F. Tsvetkov

SERIAL NO. P 0488 11/147,645	FILING DATE 06/08/2005
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The Invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
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Cree, Inc
[redacted]
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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018641/0810
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

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OFFICE NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10990607 FILING DATE: 11/17/2004
PATENT NUMBER: ISSUE DATE:
TITLE: REDUCTION OF SUBSURFACE DAMAGE IN THE PRODUCTION OF BULK SIC CRYSTALS

PAULA MCCRAY, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

11-30-06

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

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☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/990,607

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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Authorized User Name 26852

9. Signature: [redacted]

11/27/06
Date

JAMES BECHTEL
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 2

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Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Reduction of Subsurface Damage in the Production of Bulk SiC Crystals

INVENTORS(S)
Tsvetkov, Valeri
Powell, Adrian
Mueller, Stephan

SERIAL NO. P0419 10/990,607	FILING DATE 11/17/2004
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

with ______________ included in Contract No. N00014-02-C-0302

Department of the Navy (ONR)
(specify government agency).

This document confirms the paid-up license granted to the government under this contract in this invention, patent application, and any resulting patent, and all other rights acquired by the government through the referenced clause.

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Signed this 2nd day of October, 2006

ATTEST:

(Seal)

CREE, INC. CORPORATE SEAL 1987 NORTH CAROLINA

Cree, Inc
CONTRACTOR

[redacted] (b) (6)

CONTRACTOR'S OFFICIAL AND TITLE

4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECEMBER 15, 2006

PTAS

103343193A

CAROL PETROSKY
OFFICE OF NAVAL RESEARCH
OFFICE OF COUNSEL
875 NORTH RANDOLPH STREET
ARLINGTON, VA 22203-1995

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018641/0803
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
CREE INCORPORATED DOC DATE: 10/02/2006

ASSIGNEE:
NAVY, SECRETARY OF THE UNITED
STATES OF AMERICA
875 NORTH RANDOLPH STREET
OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10790406 FILING DATE: 03/01/2004
PATENT NUMBER: ISSUE DATE:
TITLE: REDUCTION OF CARROT DEFECTS IN SILICON CARBIDE EPITAXY

PAULA MCCRAY, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

11-30-06

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

12-01-2006

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Execution Date(s) 10/02/06

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☐ Security Agreement ☐ Change of Name

☐ Joint Research Agreement

☐ Government Interest Assignment

☑ Executive Order 9424, Confirmatory License

☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/790,406

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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Internal Address: OFFICE OF NAVAL RESEARCH

OFFICE OF COUNSEL

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State: VA Zip: 22203 1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Reduction of Carrot Defects in Silicon Carbide Epitaxy

INVENTORS(S)

Michael John O'Loughlin and Joseph John Sumakeris

SERIAL NO. P 0395 10/790,406	FILING DATE 03/01/2004
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

_______________ included in Contract No. N00014-02-C-0302
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ATTEST:

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CONTRACTOR

(b) (6) [redacted]

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DECEMBER 15, 2006

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018641/0757
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
CREE INCORPORATED DOC DATE: 10/02/2006

ASSIGNEE:
NAVY, SECRETARY OF THE UNITED
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875 NORTH RANDOLPH STREET
OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10929226 FILING DATE: 08/30/2004
PATENT NUMBER: ISSUE DATE:
TITLE: LITHOGRAPHIC METHODS TO REDUCE STACKING FAULT NUCLEATION SITES

PAULA MCCRAY, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

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☐ Government Interest Assignment

☑ Executive Order 9424, Confirmatory License

☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/929,226

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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7. Total fee (37 CFR 1.21(h) & 3.41) $

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Lithographic Method to Reduce Stacking Fault Nucleation Sites and Structures Having Reduced Stacking Fault Nucleation Sites

INVENTORS(S)

Joseph John Sumakeris and Mrinal Das

SERIAL NO. P 0414 10/929,226	FILING DATE 08/30/2004
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

included in Contract No. N00014-02-C-0302
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ATTEST:

(Seal)

Cree, Inc
CONTRACTOR

[redacted] (b) (6)

CONTRACTOR'S OFFICIAL AND TITLE

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DECEMBER 15, 2006

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018641/0708
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
CREE INCORPORATED DOC DATE: 10/02/2006

ASSIGNEE:
NAVY, SECRETARY OF THE UNITED
875 NORTH RANDOLPH STREET
STATES OF AMERICA, OFFICE OF NAVAL
RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10640934 FILING DATE: 08/14/2003
PATENT NUMBER: 7022378 ISSUE DATE: 04/04/2006
TITLE: NITROGEN PASSIVATION OF INTERFACE STATES IN SIO2/SIC STRUCTURES

KIMBERLY WHITE, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

12-01-2006

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☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/640,934

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Nitrogen Passivation of Interface States in SiC/SiO2 Structures

INVENTORS(S)

Das, Mrinal
Saxler, Adam

SERIAL NO. P0267	10/640,934	FILING DATE 08/14/2003
CONTRACTOR Cree, Inc		CONTRACT NO. N00014-02-C-0302

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ATTEST:

(Seal)

CREE, INC.
CORPORATE
SEAL
1987
NORTH CAROLINA

Cree, Inc

[redacted] (b) (6)

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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018641/0817
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

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875 NORTH RANDOLPH STREET
OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 10805312 FILING DATE: 03/22/2004
PATENT NUMBER: ISSUE DATE:
TITLE: BREAD MAKER AND CONTROL METHOD THEREOF

PAULA MCCRAY, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

11-30-06

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

12-01-2006

103343194

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Execution Date(s) 10/02/06

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☐ Security Agreement ☐ Change of Name

☐ Joint Research Agreement

☐ Government Interest Assignment

☑ Executive Order 9424, Confirmatory License

☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

10/805,312

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

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Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

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9. Signature: [redacted]

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Name of Person Signing

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Method to Reduce Stacking Fault Nucleation Sites and Reduce Forward Drift in Bipolar Devices

INVENTORS(S)

Sumakeris, Joseph J.

SERIAL NO. P0319 / 10/605,312	FILING DATE 09/22/2003
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The Invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

included in Contract No. N00014-02-C-0302
with

Department of the Navy (ONR).
(specify government agency)

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Signed this 2nd day of October, 2006

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(Seal)

CREE, INC.
CORPORATE
SEAL
1987
NORTH CAROLINA

Cree, Inc
CONTRACTOR

(b) (6) [redacted]

CONTRACTOR'S OFFICIAL AND TITLE

4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

DECEMBER 15, 2006

PTAS

103343190A

CAROL PETROSKY
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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018641/0789
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
CREE INCORPORATED DOC DATE: 10/02/2006

ASSIGNEE:
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875 NORTH RANDOLPH STREET
OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 11052679 FILING DATE: 02/07/2005
PATENT NUMBER: ISSUE DATE:
TITLE: PROCESS FOR PRODUCING SILICON CARBIDE CRYSTALS HAVING INCREASED MINORITY CARRIER LIFETIMES

PAULA MCCRAY, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

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4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/052,679

B. Patent No.(s)

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A. Patent Application No.(s)

11/052,679

B. Patent No.(s)

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Process for Producing Silicon Carbide Crystals Having Increased Minority Carrier Lifetimes

INVENTORS(S)

Calvin Carter, Jason Jenny, and Dave Malta

SERIAL NO. P 0475 11/052,679	FILING DATE 02/07/2005
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The Invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

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(Seal)

Cree, Inc
CONTRACTOR

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4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

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NUMBER OF PAGES: 2

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SERIAL NUMBER: 11363800 FILING DATE: 02/28/2006
PATENT NUMBER: ISSUE DATE:
TITLE: HIGH POWER SILICON CARBIDE (SIC) PIN DIODES HAVING LOW FORWARD VOLTAGE DROPS

PAULA MCCRAY, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
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11/363,800

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CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

High Power Silicon Carbide PiN Diodes Having Low Forward Voltage Drops

INVENTORS(S)
Das, Mrinal
Hull, Brett
Sumakeris, Joe

SERIAL NO. P0526 11/363,800	FILING DATE 02/28/2006
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The Invention Identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

included in Contract No. N00014-02-C-0302

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ATTEST:

(Seal)

CREE, INC. CORPORATE SEAL 1987 NORTH CAROLINA

Cree, Inc
CONTRACTOR

[redacted] (b) (6)

CONTRACTOR'S OFFICIAL AND TITLE

4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

DECEMBER 15, 2006

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CAROL PETROSKY
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RECORDATION DATE: 11/30/2006 REEL/FRAME: 018638/0303
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
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875 NORTH RANDOLPH STREET
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 11128447 FILING DATE: 05/13/2005
PATENT NUMBER: ISSUE DATE:
TITLE: METHOD AND APPARATUS FOR THE PRODUCTION OF SILICON CARBIDE CRYSTALS

JOANN STEWART, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

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4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/128,447

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

FINANCE SECTION

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY

Internal Address: OFFICE OF NAVAL RESEARCH

OFFICE OF COUNSEL

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA Zip: 22203 1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged by credit card

☐ Authorized to be charged to deposit account

☐ Enclosed

☑ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers

Expiration Date

b. Deposit Account Number CUSTOMER NUMBER

Authorized User Name 26852

9. Signature: [redacted]

Signature

11/27/06

Date

JAMES BECHTEL

Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 2

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

CREE INCORPORATED

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)

Name: NAVY, SECRETARY OF THE UNITED

Internal Address: STATES OF AMERICA

OFFICE OF NAVAL RESEARCH

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA

Country: USA Zip: 22203-1995

Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 10/02/06

- ☐ Assignment
- ☐ Merger
- ☐ Security Agreement
- ☐ Change of Name
- ☐ Joint Research Agreement
- ☐ Government Interest Assignment
- ☑ Executive Order 9424, Confirmatory License
- ☐ Other ______

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/128,447

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY

Internal Address: OFFICE OF NAVAL RESEARCH

OFFICE OF COUNSEL

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA Zip: 22203-1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

- ☐ Authorized to be charged by credit card
- ☐ Authorized to be charged to deposit account
- ☐ Enclosed
- ☑ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers ______
Expiration Date ______

b. Deposit Account Number CUSTOMER NUMBER

Authorized User Name 26852

9. Signature: (b) (6) [redacted]

Signature

11/27/06
Date

JAMES BECHTEL
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 2

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

CONFIRMATORY INSTRUMENT

APPLICATION FOR (TITLE OF INVENTION)

Method and Apparatus for the Production of Silicon Carbide Crystals

INVENTORS(S)

Valeri F. Tsvetkov and David P. Malta

SERIAL NO. P 0503 11/128,447	FILING DATE 05/13/2005
CONTRACTOR Cree, Inc	CONTRACT NO. N00014-02-C-0302

The Invention identified above is a "Subject Invention" under Patent Rights Clause 52-227-12
(identify clause by title and date)

_________________ included in Contract No. N00014-02-C-0302
with

Department of the Navy (ONR)
(specify government agency)

This document confirms the paid-up license granted to the government under this contract in this invention, patent application, and any resulting patent, and all other rights acquired by the government through the referenced clause.

The government is hereby granted an irrevocable power to inspect and make copies of the above-identified patent application.

Signed this 2nd day of October, 2006

ATTEST:

(Seal)

Cree, Inc

[redacted] (b) (6)

4600 Silicon Drive, Durham, NC 27703
BUSINESS ADDRESS

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THE ABOVE ORGANIZATION. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	c. CONTRACT NUMBER	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT *(X one)*
Cree, Inc.	N00014-02-C-0302	Same as Block 1		a. INTERIM ☐ b. FINAL ☒

b. ADDRESS *(Include ZIP Code)*	d. AWARD DATE *(YYYYMMDD)*	b. ADDRESS *(Include ZIP Code)*	d. AWARD DATE *(YYYYMMDD)*	4. REPORTING PERIOD *(YYYYMMDD)*
4600 Silicon Drive Durham, NC 27703	20020628			a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME(S) OF INVENTOR(S) *(Last, First, Middle Initial)* a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Sumakeris, Joseph; Paisley, Michael Mueller, Stephan; Hobgood, Hudson McDonald Burk, Albert	Employ Alternative Crystal Orientations to Minimize Vf Drift in Bipolar Devices	P0312 RESCIND - No Invention						

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR		g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED	
(1) (a) NAME OF INVENTOR *(Last, First, Middle Initial)*	(2) (a) NAME OF INVENTOR *(Last, First, Middle Initial)*	(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER		
(c) ADDRESS OF EMPLOYER *(Include ZIP Code)*	(c) ADDRESS OF EMPLOYER *(Include ZIP Code)*		

Contractor's [signature]
Report of Inventions and
S[redacted] 2/9/07

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" cla[redacted]

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME OF SUBCONTRACTOR(S) a.	ADDRESS *(Include ZIP Code)* b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR *(Not required if: (X as appropriate))* ☐ SMALL BUSINESS or ☐ NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL *(Last, First, Middle Initial)*	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

8

DEPARTMENT OF THE NAVY
OFFICE OF NAVAL RESEARCH
875 NORTH RANDOLPH STREET
SUITE 1425
ARLINGTON VA 22203-1995

IN REPLY REFER TO:

5870
Ser BDCC/026
February 9, 2007

From: Patent Counsel, ONR Code BDCC
To: Contracting Officer, DCMA/Raleigh Durham

Subj: CONTRACT NUMBER N00014-02-C-0302 WITH CREE INCORPORATED

Encl: (1) DD Form 882 dated October 2, 2006

1. Enclosed is the above Contractor's final Report of Inventions and Subcontracts.

2. The Contractor has fulfilled all the patent requirements of the Contract; therefore, patent clearance is granted.

[redacted]
JA[redacted]
Patent Counsel of the Navy

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THE ABOVE ORGANIZATION. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR: Cree, Inc.	c. CONTRACT NUMBER: N00014-02-C-0302	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR: Same as Block 1	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one): a. INTERIM / X b. FINAL
b. ADDRESS (Include ZIP Code): 4600 Silicon Drive, Durham, NC 27703	d. AWARD DATE (YYYYMMDD): 20020628	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD): a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Tsvetkov, Valeri Brady, Mark	Reduction of Cracking Rate in SiC	P0383		X		X		X

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR		g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED	
(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER		
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)		

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached							

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) ☐ SMALL BUSINESS or ☐ NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted] (b) (6)	10/2/06

DD FORM 882, JUL 2005 PREVIOUS EDITION IS OBSOLETE

CCR 050007 1031

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
Carnegie Melon University	5000 Forbes Avenue Pittsburgh, PA 15213-3890	02-005	52.227-11	Jan-97	Characterization services	20020628	20040627
Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Aug 31, 2001

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THIS ADDRESS. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	c. CONTRACT NUMBER	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one)
Cree, Inc	N00014-02-C-0302	Same as 1a	Same as 1c	a. INTERIM / b. FINAL: X

b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD)
4600 Silicon Drive Durham, NC 27703	20020628	Same as 1b	Same as 1d	a. FROM 20020528 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Michael Laughner, Jack Clayton	Chemical Mechanical Polish (CMP) of Silicon Carbide surfaces	P0380 RESCIND - No Invention						

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR		g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED	
(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER		
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)		

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) SMALL BUSINESS or NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

CCH 090336 1231

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to the Department of Defense, Executive Services Directorate (9000-0095). Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THE ABOVE ORGANIZATION. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR: Cree, Inc.

c. CONTRACT NUMBER: N00014-02-C-0302

2.a. NAME OF GOVERNMENT PRIME CONTRACTOR: Same as 1a

c. CONTRACT NUMBER: Same as 1c

3. TYPE OF REPORT (X one): a. INTERIM [ ] b. FINAL [X]

b. ADDRESS (Include ZIP Code): 4600 Silicon Drive, Durham, NC 27703

d. AWARD DATE (YYYYMMDD): 20020628

b. ADDRESS (Include ZIP Code): Same as 1b

d. AWARD DATE (YYYYMMDD): 20020628

4. REPORTING PERIOD (YYYYMMDD): a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Sumakeris, Joseph J. Das, Mrinal	Lithographic Method to Reduce Stacking Fault Nucleation Sites and Structures Having Reduced Stacking Fault Nucleation Sites	P0 414	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)

(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)

(b) NAME OF EMPLOYER

(b) NAME OF EMPLOYER

(c) ADDRESS OF EMPLOYER (Include ZIP Code)

(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION

(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached.							

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) [ ] SMALL BUSINESS or [ ] NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial): Degnan, Sharon M

b. TITLE: Contracts Manager

c. SIGNATURE: [redacted]

d. DATE SIGNED: 10/2/02

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
Carnegie Melon University	5000 Forbes Avenue Pittsburgh, PA 15213-3890	02-005	52.227-11	Jan-97	Characterization services	20020628	20040627
Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

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1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	Cree, Inc.
c. CONTRACT NUMBER	N00014-02-C-0302
b. ADDRESS (Include ZIP Code)	4600 Silicon Drive Durham, NC 27703
d. AWARD DATE (YYYYMMDD)	20020628
2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	Same as 1a
c. CONTRACT NUMBER	Same as 1c
b. ADDRESS (Include ZIP Code)	Same as 1b
d. AWARD DATE (YYYYMMDD)	20020628
3. TYPE OF REPORT (X one)	a. INTERIM ☐ b. FINAL ☒
4. REPORTING PERIOD (YYYYMMDD)	a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Carter, Calvin Jenny, Jason Malta, Dave	Process for Producing Silicon Carbide Crystals Having Increased Minority Carrier Lifetimes	P0 475	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached							

SECTION III - CERTIFICATION

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

DD FORM 882, JUL 2005 PREVIOUS EDITION IS OBSOLETE. FormFlow/Adobe Professional 6.0

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
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Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
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Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS
(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THE ABOVE ORGANIZATION. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	c. CONTRACT NUMBER	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one)
Cree, Inc.	N00014-02-C-0302	Same as 1a	Same as 1c	a. INTERIM; X b. FINAL
b. ADDRESS (Include ZIP Code) 4600 Silicon Drive Durham, NC 27703	d. AWARD DATE (YYYYMMDD) 20020628	b. ADDRESS (Include ZIP Code) Same as 1b	d. AWARD DATE (YYYYMMDD) 20020628	4. REPORTING PERIOD (YYYYMMDD) a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	d. ELECTION TO FILE PATENT APPLICATIONS (X): (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	e. CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X): (a) YES	(b) NO
Sumakeris, Joesph	Silicon Carbice Semiconductor Structures Including Multiple Epitaxial Layers Having Sidewalls (as amended)	P0477	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1)	(2)
(a) NAME OF INVENTOR (Last, First, Middle Initial): Hallin Christer	(a) NAME OF INVENTOR (Last, First, Middle Initial): Ledenmann, Heinz
(b) NAME OF EMPLOYER: ABB	(b) NAME OF EMPLOYER: ABB
(c) ADDRESS OF EMPLOYER (Include ZIP Code): Sweden	(c) ADDRESS OF EMPLOYER (Include ZIP Code): Sweden

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	d. FAR "PATENT RIGHTS" (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	f. SUBCONTRACT DATES (YYYYMMDD) (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached							

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) SMALL BUSINESS or NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Deguan, Sharon M	Contracts Manager	[redacted] (b) (6)	10/2/02

DD FORM 882, JUL 2005 PREVIOUS EDITION IS OBSOLE[redacted] FormFlow/Adobe Professional 6.0

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

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Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS

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Cree, Inc.	N00014-02-C-0302	Same as 1a	Same as 1c	a. INTERIM / X b. FINAL

b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD)
4600 Silicon Drive Durham, NC 27703	20020628	Same as 1b	20020628	a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

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NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	e. (b) NO
Das, Mrinal Hull, Brett Sumakeris, Joe	High Power Silicon Carbide PiN Diodes Having Low Forward Voltage Drops	P0526	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached							

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted] (b) (6)	10/2/02

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ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

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Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS
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Cree, Inc.	N00014-02-C-0302	Same as Block 1		a. INTERIM; X b. FINAL
b. ADDRESS (Include ZIP Code) 4600 Silicon Drive Durham NC 27703	d. AWARD DATE (YYYYMMDD) 20020628	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD) a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

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NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Tsvetkov, Valeri Brady, Mark	Bulk Silicon Carbide Single Crystal Growth without Polycrystalline Rim	P0384		X		X		X

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
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(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

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(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

CCH 050007 1031

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

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Contract Number: N00014-02-C-0302

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Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS

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b. ADDRESS (Include ZIP Code): 4600 Silicon Drive, Durham, NC 27703	d. AWARD DATE (YYYYMMDD): 20020628	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD): a. FROM 20020628 b. TO 20050222

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NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	d. ELECTION TO FILE PATENT APPLICATIONS (X) (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	e. CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) (a) YES	(b) NO
Tsvetkov, Valeri Powell, Adrian Mueller, Stephan	Reduction of Subsurface Damage in the Production of Bulk SiC Crystals	10/990,607	x			x	X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR	g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED
(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)
(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	d. FAR "PATENT RIGHTS" (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	f. SUBCONTRACT DATES (YYYYMMDD) (1) AWARD	(2) ESTIMATED COMPLETION
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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	~~20050913~~ 10/2/06

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ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

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Contract Number: N00014-02-C-0302

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Cree, Inc.	N00014-02-C-0302	Same as 1a	Same as 1c	a. INTERIM [ ] b. FINAL [X]

b. ADDRESS *(Include ZIP Code)*	d. AWARD DATE *(YYYYMMDD)*	b. ADDRESS *(Include ZIP Code)*	d. AWARD DATE *(YYYYMMDD)*	4. REPORTING PERIOD *(YYYYMMDD)*
4600 Silicon Drive Durham, NC 27703	20020628	Same as 1b	20020628	a. FROM 20020628 b. TO 20050222

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Powell, Adrian Brady, Mark Tsvetkov, Valeri F.	Low basal plane dislocation bulk grown SiC wafers	P0 488	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR *(Last, First, Middle Initial)*	(2) (a) NAME OF INVENTOR *(Last, First, Middle Initial)*
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER *(Include ZIP Code)*	(c) ADDRESS OF EMPLOYER *(Include ZIP Code)*

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SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

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Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

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Tvsetkov, Valeri F. Malta, David P.	Method and Apparatus for the Production of Silicon Carbide Crystals	P0 503	X		X		X	

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(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER		
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)		

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

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SECTION III - CERTIFICATION

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I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M.	Contracts Manager	(b) (6) [redacted]	10/2/06

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
Carnegie Melon University	5000 Forbes Avenue Pittsburgh, PA 15213-3890	02-005	52.227-11	Jan-97	Characterization services	20020628	20040627
Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS
(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

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PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THE ABOVE ORGANIZATION. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	Cree, Inc.
c. CONTRACT NUMBER	N00014-02-C-0302
2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	Same as 1a
c. CONTRACT NUMBER	Same as 1c
3. TYPE OF REPORT (X one)	a. INTERIM; X b. FINAL
b. ADDRESS (Include ZIP Code)	4600 Silicon Drive Durham, NC 27703
d. AWARD DATE (YYYYMMDD)	20020628
b. ADDRESS (Include ZIP Code)	Same as 1b
d. AWARD DATE (YYYYMMDD)	20020628
4. REPORTING PERIOD (YYYYMMDD)	a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Das, Mrinal Saxler, Adam	Nitrogen Passivation of Interface States in SiC SiO2 Structures	P0267	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached							

SECTION III - CERTIFICATION

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M.	Contracts Manager	[redacted]	10/2/06

DD FORM 882, JUL 2005 PREVIOUS EDITION IS OBSO[redacted] FormFlow/Adobe Professional 6.0

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
Carnegie Melon University	5000 Forbes Avenue Pittsburgh, PA 15213-3890	02-005	52.227-11	Jan-97	Characterization services	20020628	20040627
Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette. IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS
(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved
OMB No. 9000-0095
Expires Jan 31, 2008

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1.a. NAME OF CONTRACTOR/SUBCONTRACTOR: Cree, Inc.
c. CONTRACT NUMBER: N00014-02-C-0302
b. ADDRESS (Include ZIP Code): 4600 Silicon Drive, Durham, NC 27703
c. AWARD DATE (YYYYMMDD): 20020628

2.a. NAME OF GOVERNMENT PRIME CONTRACTOR: Same as 1a
c. CONTRACT NUMBER: Same as 1c
b. ADDRESS (Include ZIP Code): Same as 1b
d. AWARD DATE (YYYYMMDD): 20020628

3. TYPE OF REPORT (X one): a. INTERIM | X b. FINAL

4. REPORTING PERIOD (YYYYMMDD): a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Ryu, Sei-Hyung	Vertical JFET Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors and Methods of Fabricating Vertical JFET Limited Silicon Carbide Metal-Oxide Semi-conductor Field Effect Transistors	P0 279	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR
(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)
(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED
(1) TITLE OF INVENTION
(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
Please see attached							

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) SMALL BUSINESS or NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial): Degnan, Sharon M
b. TITLE: Contracts Manager
c. SIGNATURE: [redacted]
d. DATE SIGNED: 10/2/06

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
Carnegie Melon University	5000 Forbes Avenue Pittsburgh, PA 15213-3890	02-005	52.227-11	Jan-97	Characterization services	20020628	20040627
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Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Jan 31, 2008

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	c. CONTRACT NUMBER	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one)
Cree, Inc.	N00014-02-C-0302	Same as Ia	Same as 1c	a. INTERIM / X b. FINAL
b. ADDRESS (Include ZIP Code) 4600 Silicon Drive Durham, NC 27703	d. AWARD DATE (YYYYMMDD) 20020628	b. ADDRESS (Include ZIP Code) Same as 1b	d. AWARD DATE (YYYYMMDD) 20020628	4. REPORTING PERIOD (YYYYMMDD) a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	e. (b) NO
Sumakeris, Joseph J. Paisley, Michael P. O'Loughlin, Michael J.	Methods and Apparatus for Controlling Formation of Deposits in a Deposition System and Deposition Systems and Methods Including the Same	P0 297	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
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SECTION III - CERTIFICATION

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

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Case Western University	10900 Euclid Avenue Cleveland OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS
(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

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c. CONTRACT NUMBER	N00014-02-C-0302
b. ADDRESS (Include ZIP Code)	4600 Silicon Drive Durham, NC 27703
d. AWARD DATE (YYYYMMDD)	20020628
2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	Same as 1a
c. CONTRACT NUMBER	Same as 1c
b. ADDRESS (Include ZIP Code)	Same as 1b
d. AWARD DATE (YYYYMMDD)	20020628
3. TYPE OF REPORT (X one)	a. INTERIM [ ] b. FINAL [X]
4. REPORTING PERIOD (YYYYMMDD)	a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

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NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
Sumakeris, Joseph	Method to Reduce Stacking Fault Nucleation Sites and Reduce Forward Voltage Drift in Bipolar Devices	P0319/P0319US2	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)

(b) NAME OF EMPLOYER

(c) ADDRESS OF EMPLOYER (Include ZIP Code)

(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)

(b) NAME OF EMPLOYER

(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION

(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
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SECTION III - CERTIFICATION

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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Degnan, Sharon M	Contracts Manager	[redacted]	10/2/06

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

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REPORT OF INVENTIONS AND SUBCONTRACTS

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b. ADDRESS (Include ZIP Code): 4600 Silicon Drive, Durham, NC 27703	d. AWARD DATE (YYYYMMDD): 20020628	b. ADDRESS (Include ZIP Code): Same as 1b	d. AWARD DATE (YYYYMMDD): 20020628	4. REPORTING PERIOD (YYYYMMDD): a. FROM 20020628 b. TO 20050222

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NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	e. (b) NO
Sumakeris, Joseph J. O'Loughlin, Michael J.	Reduction of Carrot Defects in Silicon Carbide Epitaxy	P0 395	X		X		X	

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	d. (2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	f. (2) ESTIMATED COMPLETION
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a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial): Degnan, Sharon M	b. TITLE: Contract Manager	c. SIGNATURE: [redacted]	d. DATE SIGNED: 10/2/02

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

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Purdue University	302 Wood Street West Lafayette, IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

REPORT OF INVENTIONS AND SUBCONTRACTS
(Pursuant to "Patent Rights" Contract Clause) (See instructions on back)

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1.a. NAME OF CONTRACTOR/SUBCONTRACTOR Cree, Inc.	c. CONTRACT NUMBER N00014-02-C-0302	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR Same as Block 1	c. CONTRACT NUMBER	3. TYPE OF REPORT *(X one)* a. INTERIM X b. FINAL
b. ADDRESS *(Include ZIP Code)* 4600 Silicon Drive Durham, NC 27703	d. AWARD DATE *(YYYYMMDD)* 20020628	b. ADDRESS *(Include ZIP Code)*	d. AWARD DATE *(YYYYMMDD)*	4. REPORTING PERIOD *(YYYYMMDD)* a. FROM 20020628 b. TO 20050222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME(S) OF INVENTOR(S) *(Last, First, Middle Initial)* a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
O'Loughlin, Michael	Excess Silane Abatement Device	P0396		X		X		X

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR *(Last, First, Middle Initial)*

(b) NAME OF EMPLOYER

(c) ADDRESS OF EMPLOYER *(Include ZIP Code)*

(2) (a) NAME OF INVENTOR *(Last, First, Middle Initial)*

(b) NAME OF EMPLOYER

(c) ADDRESS OF EMPLOYER *(Include ZIP Code)*

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION

(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS *(Containing a "Patent Rights" clause)*

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR *(If "None," so state)*

NAME OF SUBCONTRACTOR(S) a.	ADDRESS *(Include ZIP Code)* b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR *(Not required if: (X as appropriate))* SMALL BUSINESS or NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL *(Last, First, Middle Initial)* Degnan, Sharon M	b. TITLE Contracts Manager	c. SIGNATURE (b) (6) [redacted]	d. DATE SIGNED 10/2/06

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CCH 050007 1011

ATTACHMENT TO REPORT OF INVENTIONS AND SUBCONTRACTS

Prime Contractor: Cree, Inc.
Contract Number: N00014-02-C-0302

6. Subcontracts Awarded by Contractor/Subcontractor

Name of Subcontractor(s)	Address	Subcontract Number	FAR "Patent Rights" Clause	FAR "Patent Rights" Date	Description of Work to be Performed	Subcontract Dates Award	Subcontract Dates Est. Compl.
Carnegie Melon University	5000 Forbes Avenue Pittsburgh, PA 15213-3890	02-005	52.227-11	Jan-97	Characterization services	20020628	20040627
Case Western University	10900 Euclid Avenue Cleveland, OH 44106-7015	02-006	52.227-12	Jan-97	Substrate Material and Device Structures	20020628	20041128
Purdue University	302 Wood Street West Lafayette IN 47907	02-007	52.227-11	Jan-97	Dev. High Power SiC MOSFETs	20020628	20041222
Rensselaer	110 8th Street Troy, NY 12180	04-001	52.227-11	Jan-97	Evaluation of Sic Substrates	20040201	20041222

Ref: 9204._1040187 CMU

REPORT OF INVENTIONS AND SUBCONTRACTS

(PURSUANT TO "PATENT RIGHTS" CONTRACT CLAUSE) (SEE INSTRUCTIONS ON REVERSE SIDE)

FORM APPROVED
OMB NO. 0704-0297
EXPIRES JUNE 30, 1992

1a. NAME OF CONTRACTOR/SUBCONTRACTOR CARNEGIE MELLON UNIVERSITY	c. CONTRACT NUMBER 02-005	2a. NAME OF GOVERNMENT PRIME CONTRACTOR CREE, INC	c. CONTRACT NUMBER N00014-02-C-0302	3. TYPE OF REPORT (X ONE) INTERIM / X FINAL
b. ADDRESS (INCLUDE ZIP CODE) 5000 FORBES AVENUE PITTSBURGH, PA 15213-3890	d. AWARD DATE (YYMMDD)	b. ADDRESS (INCLUDE ZIP CODE)	d. AWARD DATE (YYMMDD)	4. REPORTING PERIOD (YYMMDD) a. FROM 02/05/28 b. TO 04/05/28

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (IF "NONE" SO STATE)

a. NAMES OF INVENTOR(S) LAST, FIRST, MI	b. TITLE OF INVENTION(S)	c. DISCLOSURE NUMBER PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER	d. ELECTION TO FILE PATENT APPLICATIONS (1) U.S. (a) YES	(1) U.S. (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	e. CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (1) YES	(2) NO
	NONE							

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR		g. ELECTED FOREIGN COUNTRIES IN WHICH A FOREIGN PATENT APPLICATION WILL BE FILED	
(1)(a) NAME OF INVENTOR (LAST, FIRST, MI)	(2)(a) NAME OF INVENTOR (LAST, FIRST, MI)	(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER	NONE	
(c) ADDRESS OF EMPLOYER (INCLUDE ZIP CODE)	(c) ADDRESS OF EMPLOYER (INCLUDE ZIP CODE)		

SECTION II - SUBCONTRACTS (CONTAINING A "PATENT RIGHTS" CLAUSE)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (IF "NONE" SO STATE)

a. NAME OF SUBCONTRACTORS	b. ADDRESS (INCLUDE ZIP CODE)	c. SUBCONTRACT NO.(S)	d. DFAR "PATENT RIGHTS" (1) CLAUSE NUMBER	(2) DATE (YYMM)	e. DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S)	f. SUBCONTRACT DATES (YYMMDD) (1) AWARD	(2) ESTIMATED COMPLETION
		NONE					

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR NOT REQUIRED IF SMALL BUSINESS X | NON-PROFIT ORGANIZATION (X APPROPRIATE BOX)

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL Susan Burkett	c. I CERTIFY THAT THE REPORTING PARTY HAS PROCEDURES FOR PROMPT IDENTIFICATION AND TIMELY DISCLOSURE OF SUBJECT INVENTIONS, THAT SUCH PROCEDURES HAVE BEEN FOLLOWED AND THAT ALL SUBJECT INVENTIONS HAVE BEEN REPORTED.	
b. TITLE Associate Provost	d. SIGNATURE [redacted]	e. DATE SIGNED 04/11/12

Form Approved
OMB No. 9000-0095
Expires Jan 31, 2008

REPORT OF INVENTIONS AND SUBCONTRACTS
(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to the Department of Defense, Executive Services Directorate (9000-0095). Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THE ABOVE ORGANIZATION. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR: Case Western Reserve Univer.	c. CONTRACT NUMBER: 02-006	
b. ADDRESS (Include ZIP Code): 10900 Euclid Ave. Cleveland, Ohio 44106-7015	d. AWARD DATE (YYYYMMDD): 20020701	
2.a. NAME OF GOVERNMENT PRIME CONTRACTOR: Cree, Inc.	c. CONTRACT NUMBER: N00014-02-C-0302	3. TYPE OF REPORT (X one): a. INTERIM; X b. FINAL
b. ADDRESS (Include ZIP Code): 4600 Silicon Drive, Durham, NC 27703	d. AWARD DATE (YYYYMMDD): 20020628	4. REPORTING PERIOD (YYYYMMDD): a. FROM 20020628; b. TO 20041128

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
None.								

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION
None.							

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) SMALL BUSINESS or ✓ NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
DEREK M. HUMPHREY	Assistant Director Sponsored Projects Administration Case Western Reserve University	[redacted]	09-26-2006

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REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on Reverse Side.)

Form Approved OMB No. 9000-0095 Expires Aug 31, 2001

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	c. CONTRACT NUMBER	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one)
Purdue University	02-007	Office of Naval Research	NDARPA BAA 01-35	a. INTERIM / X b. FINAL
b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD)
610 Purdue Mall, Room 300 West Lafayette IN 47907-2040	20020628			a. FROM 20020628 b. TO 20041222

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) United States (a) Yes	(1) United States (b) No	(2) Foreign (a) Yes	(2) Foreign (b) No	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) Yes	e. (b) No
	NONE							

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR

(1)(a) Name of Inventor (Last, First, Middle Initial)

(2)(a) Name of Inventor (Last, First, Middle Initial)

(b) Name of Employer

(b) Name of Employer

(c) Address of Employer (Include ZIP Code)

(c) Address of Employer (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) Title of Invention

(2) Foreign Countries of Patent Application

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) Clause Number	d. (2) Date (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) Award	f. (2) Estimated Completion
NONE							

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) Small Business or | Non-Profit organization (X appropriate box)

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR Official (Last, First, Middle Initial)	b. TITLE Special Assistant to the Vice Provost for Research	c. SIGNATURE	d. DATE SIGNED
Baitinger, William E.	Special Asst. to the V. P. for Research	[redacted]	9/15/05

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on back)

Form Approved OMB No. 9000-0095 Expires Oct 31, 2004

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO THIS ADDRESS. RETURN COMPLETED FORM TO THE CONTRACTING OFFICER.

1.a. NAME OF CONTRACTOR/SUBCONTRACTOR	c. CONTRACT NUMBER	2.a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one)
Rensselaer Polytechnic Institute				a. INTERIM / X b. FINAL
b. ADDRESS (Include ZIP Code) 110 Eighth Street, Troy, New York 12180	d. AWARD DATE (YYYYMMDD) 11/1/04	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYYYMMDD)	4. REPORTING PERIOD (YYYYMMDD) a. FROM 11/1/04 b. TO 12/22/04

SECTION I - SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME(S) OF INVENTOR(S) (Last, First, Middle Initial) a.	TITLE OF INVENTION(S) b.	DISCLOSURE NUMBER, PATENT APPLICATION SERIAL NUMBER OR PATENT NUMBER c.	ELECTION TO FILE PATENT APPLICATIONS (X) d. (1) UNITED STATES (a) YES	(1) UNITED STATES (b) NO	(2) FOREIGN (a) YES	(2) FOREIGN (b) NO	CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (X) e. (a) YES	(b) NO
N/A	N/A	N/A						

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR/SUBCONTRACTOR		g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED	
(1) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(2) (a) NAME OF INVENTOR (Last, First, Middle Initial)	(1) TITLE OF INVENTION	(2) FOREIGN COUNTRIES OF PATENT APPLICATION
(b) NAME OF EMPLOYER	(b) NAME OF EMPLOYER		
(c) ADDRESS OF EMPLOYER (Include ZIP Code)	(c) ADDRESS OF EMPLOYER (Include ZIP Code)		

SECTION II - SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR/SUBCONTRACTOR (If "None," so state)

NAME OF SUBCONTRACTOR(S) a.	ADDRESS (Include ZIP Code) b.	SUBCONTRACT NUMBER(S) c.	FAR "PATENT RIGHTS" d. (1) CLAUSE NUMBER	(2) DATE (YYYYMM)	DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S) e.	SUBCONTRACT DATES (YYYYMMDD) f. (1) AWARD	(2) ESTIMATED COMPLETION

SECTION III - CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR/SUBCONTRACTOR (Not required if: (X as appropriate)) SMALL BUSINESS or NONPROFIT ORGANIZATION

I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.

a. NAME OF AUTHORIZED CONTRACTOR/SUBCONTRACTOR OFFICIAL (Last, First, Middle Initial)	b. TITLE	c. SIGNATURE	d. DATE SIGNED
Richard E. Scammell	Director, Research Administration & Finance	(b) (6) [redacted]	9/28/06

CONTRACT COMPLETION STATEMENT

1. FROM: *(Contract Administration Office)* DCM Atlanta 805 Walker St., Suite 1 Marietta, Ga	2a. PII NUMBER N00014-02C0302 2b. LAST MODIFICATION NUMBER ~~P00007~~ P00007 2c. CALL/ORDER NUMBER
3. TO: *(Name and Address of Purchasing Office and Office Symbol of the PCO, if known)* ONE LIBERTY CENTER Office of Naval Research Code 25, FL12 Arlington, Va. 22203-1995	4. CONTRACTOR IDENTITY CODE AND ADDRESS Cree Inc., 0C9J8 5. EXCESS FUNDS ☐ YES ☒ NO $

6a. IF FINAL PAYMENT HAS BEEN MADE, COMPLETE ITEMS 6b., AND 6c.	6b. VOUCHER NUMBER 000000	6c. DATE 9/26/07
7a. IF FINAL APPROVED INVOICE FORWARDED TO D.O. OF ANOTHER ACTIVITY AND STATUS OF PAYMENT IS UNKNOWN, COMPLETE ITEMS 7b, and 7c.	7b. INVOICE NUMBER	7c. DATE FORWARDED

8. REMARKS

"Excess funds to de-obligate (ULO is $0)"

"Physical Completion Date is 2/7/05"

9a. ALL ADMINISTRATION OFFICE ACTIONS REQUIRED HAVE BEEN FULLY AND SATISFACTORILY ACCOMPLISHED. THIS INCLUDES FINAL SETTLEMENT IN THE CASE OF A PRICE REVISION CONTRACT

9b. TYPED NAME OF RESPONSIBLE OFFICIAL	9c. SIGNATURE	9d. DATE 9/27/07

FOR PURCHASING OFFICE USE ONLY

10a. ALL PURCHASING OFFICE ACTIONS REQUIRED HAVE BEEN FULLY AND SATISFACTORILY ACCOMPLISHED. CONTRACT FILE OF THIS OFFICE IS HEREBY CLOSED AS OF:

☐ DATE SHOWN IN ITEM 9d. ABOVE.

☒ DATE SHOWN IN ITEM 10e. BELOW. *(Check this box only if final completion of any significant purchasing office action extends more than three months beyond close-out date shown in item 9d. above. In such cases, submit a copy of the completed form upon final accomplishment of all purchasing office actions to the contract administration office. (Upon receipt, the contract administration office shall extend its contract file close-out date accordingly.))*

10b. REMARKS

In accordance with the PK-9 REPORT dated September 2007 attached. Contract number N00014 02C0302 was closed by DCMA ACO on 9/27/07.

prepared by Pr.tech

10c. TYPED NAME OF RESPONSIBLE OFFICIAL	10d. SIGNATURE	10e. DATE
ELLEN SIMONOFF CONTRACTING OFFICER	(b) (6) [redacted]	6-14-10

DD FORM 1594, FEB 70 Replaces edition of 1 JU[redacted] which is obsolete. Adobe Professional 7.0